

Model Name:GA-G31M-ES2L

Revision 1.11

SHEET

TITLE

01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4 LGA775 A
05	P4 LGA775 B,D
06	P4 LGA775 C
07	P4 LGA775 E,F,G,H
08	G31 HOST
09	G31 DDRII
10	G31 PCI E, DMI
11	G31 VGA
12	G31 GND
13	G31 PWR
14	PCI EXPRESS*16 SLOT
15	DDRII CHANNEL A
16	DDRII CHANNEL B
17	DDRII TERMINATION
18	ICH7 PCI, USB, DMI, LAN
19	ICH7 IDE, GPIO, SATA, CTRL
20	ICH7 VCC, GND
21	CK505 CLOCK.
22	PCI SLOT 1,2,PCIE*1
23	IDE/FLOPPY
24	ITE 8718 GB/HX
25	COM LPT
26	CI,HWM,KB/MS,DUALBIOS
27	ALC883

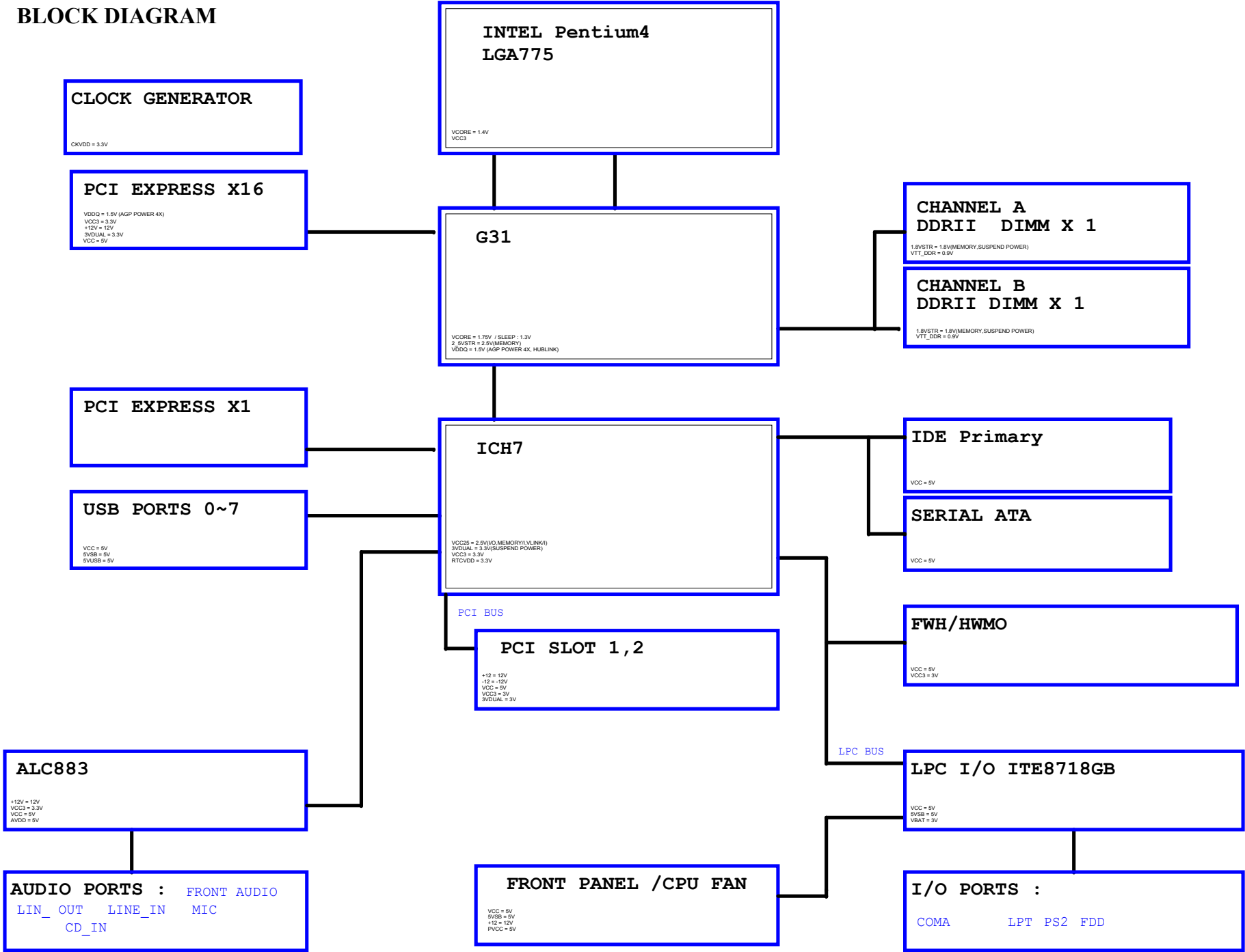
SHEET

TITLE

28	REAR AUDIO JACK
29	DISCRETE POWER
30	VCORE PWM ISL6312
31	ATX, OTHERS POWER
32	FRONT PANEL
33	REALTEK RTL8111C/8102E

Gigabyte Technology			
Title			
Cover Sheet			
Size	Document Number	GA-G31M-ES2L	Rev
Custom			1.11
Date:	Thursday, July 17, 2008	Sheet	1 of 33

BLOCK DIAGRAM

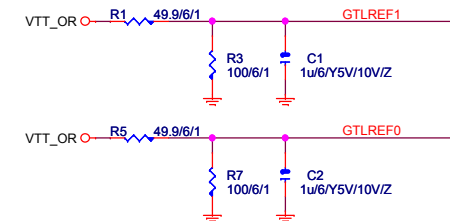
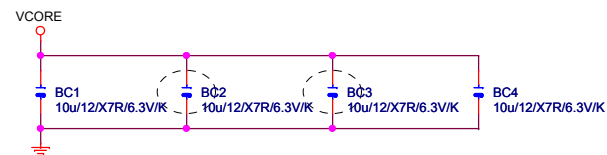
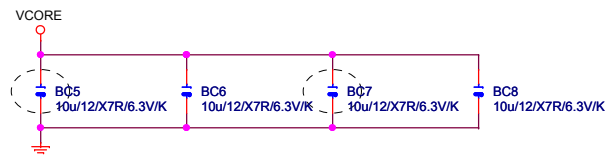


Version: 1.11

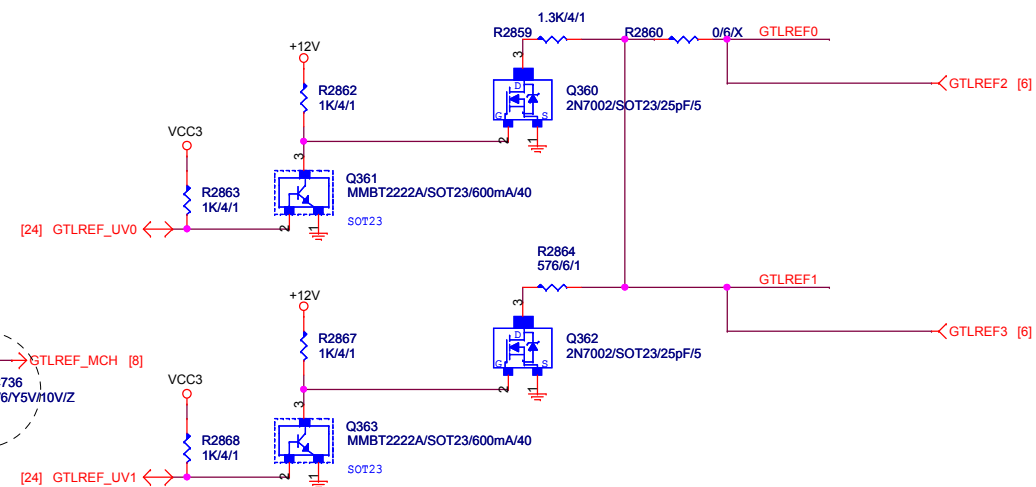
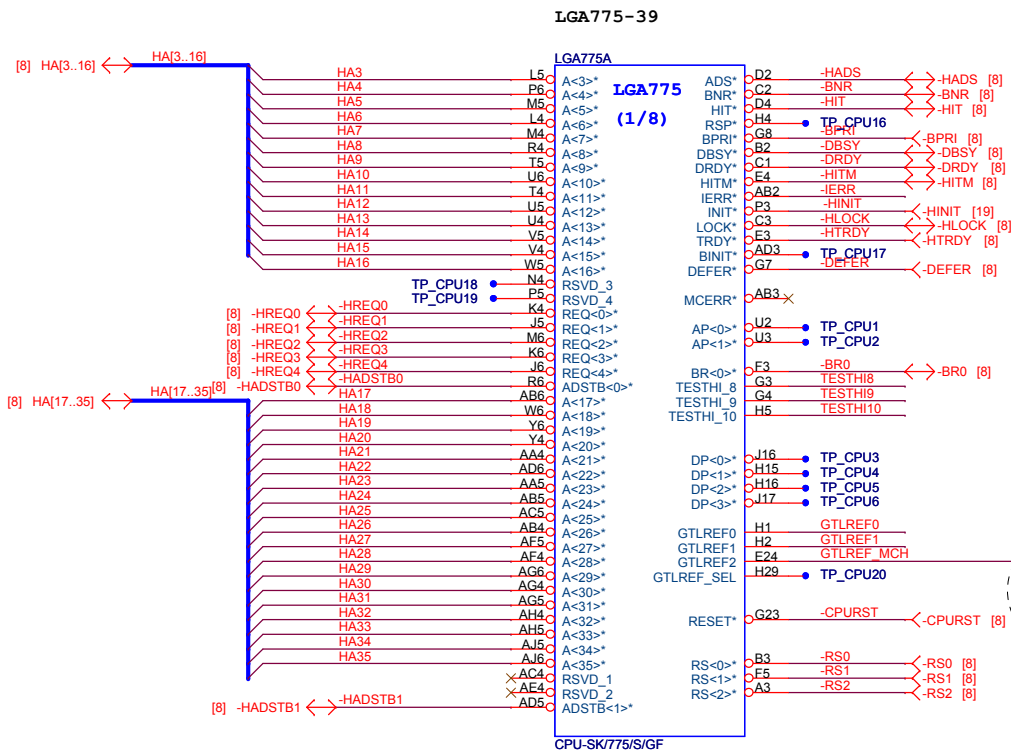
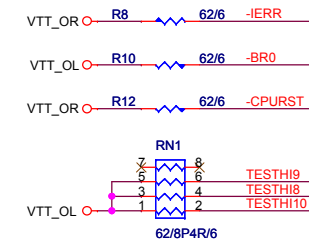
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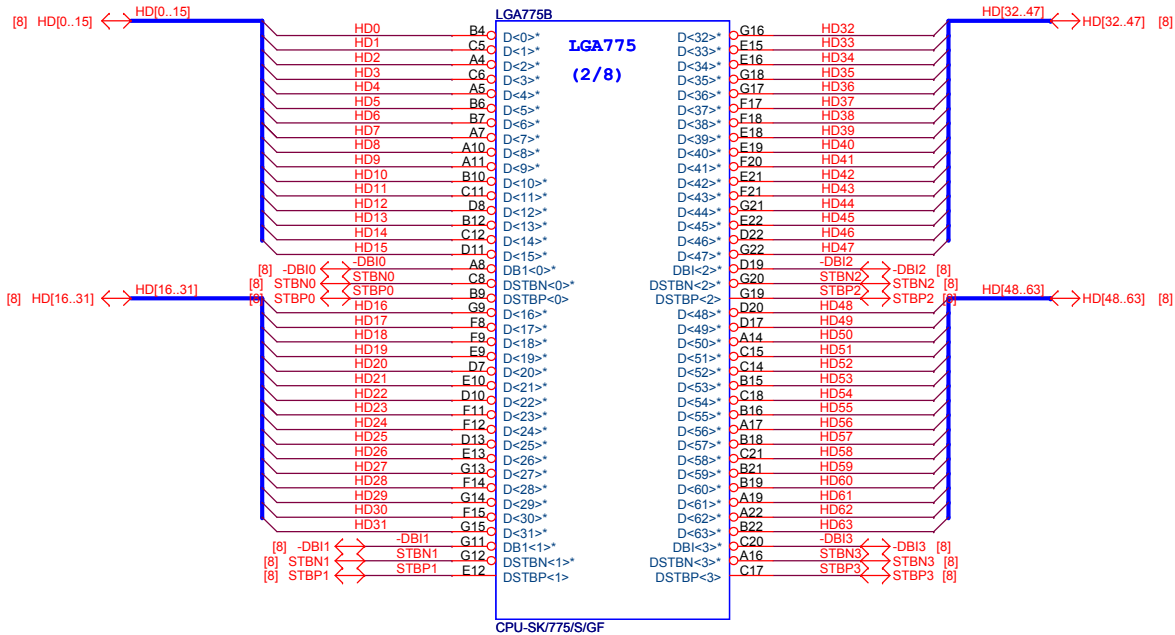
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<i>Gigabyte Technology</i>			
BOM & PCB MODIFY HISTORY			
Size Custom	Document Number	GA-G31M-ES2L	Rev 1.1
Date: Friday, July 18, 2008		Sheet 3 of 33	

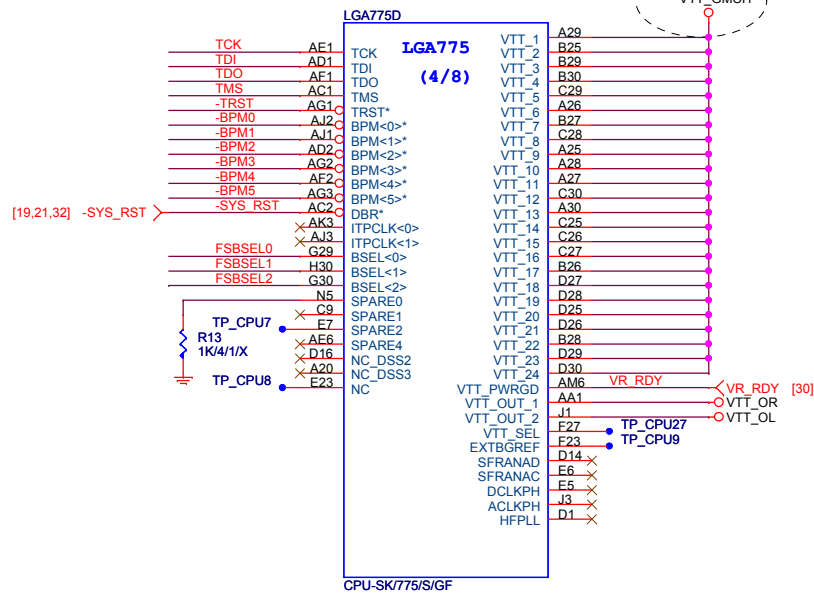


中間値0.9V

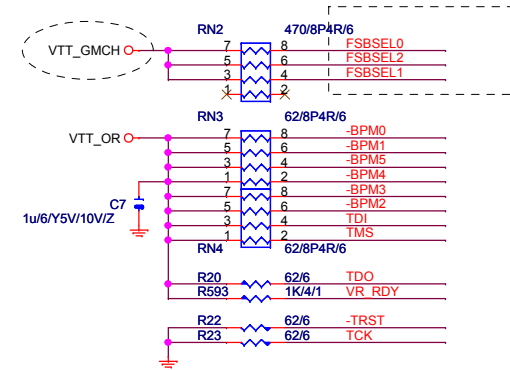




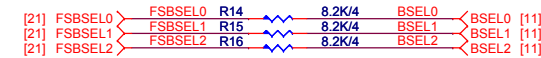
CPU-SK/775/S/GF



CPU-SK/775/S/GF



TO CLK GEN

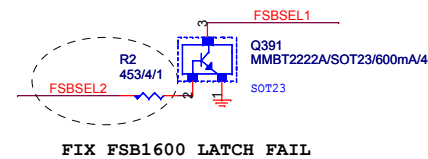


TO NB

CPU

NA	FSB	FSA	
FSBSEL3	FSBSEL1	FSBSEL0	Clock
1	0	1	100MHz
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
0	0	0	266MHz

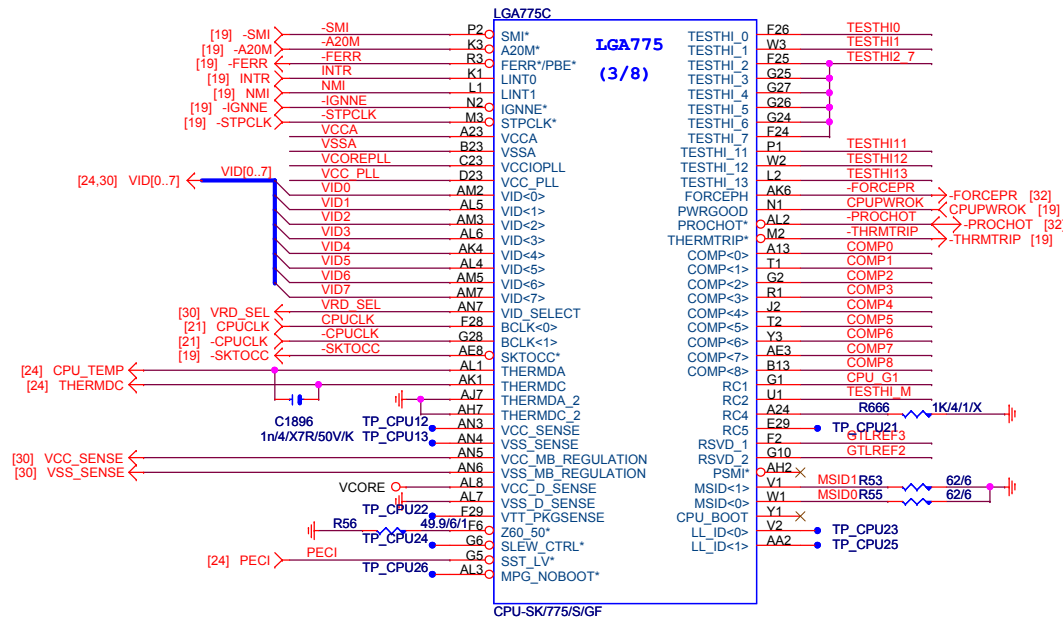
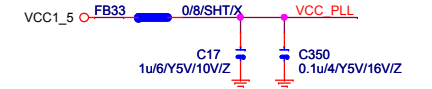
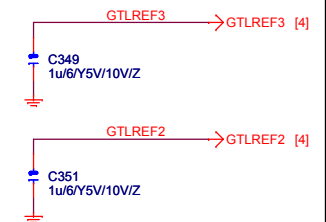
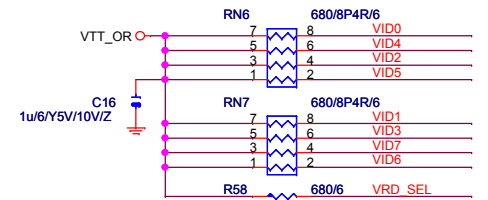
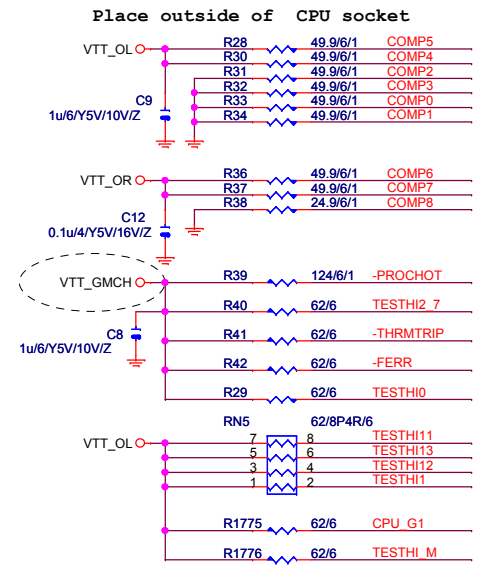
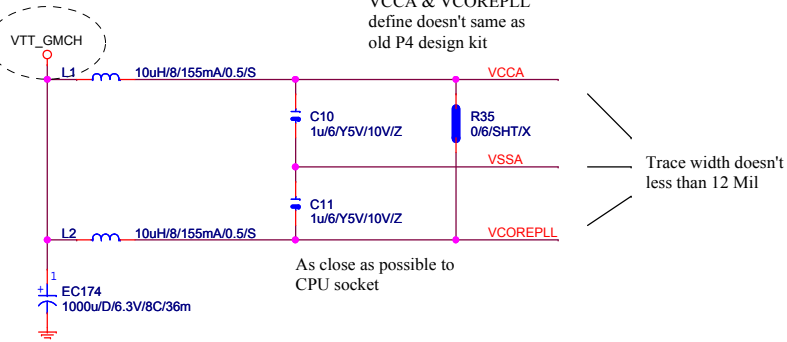
X



FIX FSB1600 LATCH FAIL

<div>Gigabyte Technology</div>			
Title			
P4_LGA775-B,D			
Size B	Document Number		Rev
	GA-G31M-ES2L		1.11
Date:	Thursday, July 17, 2008	Sheet	5 of 33

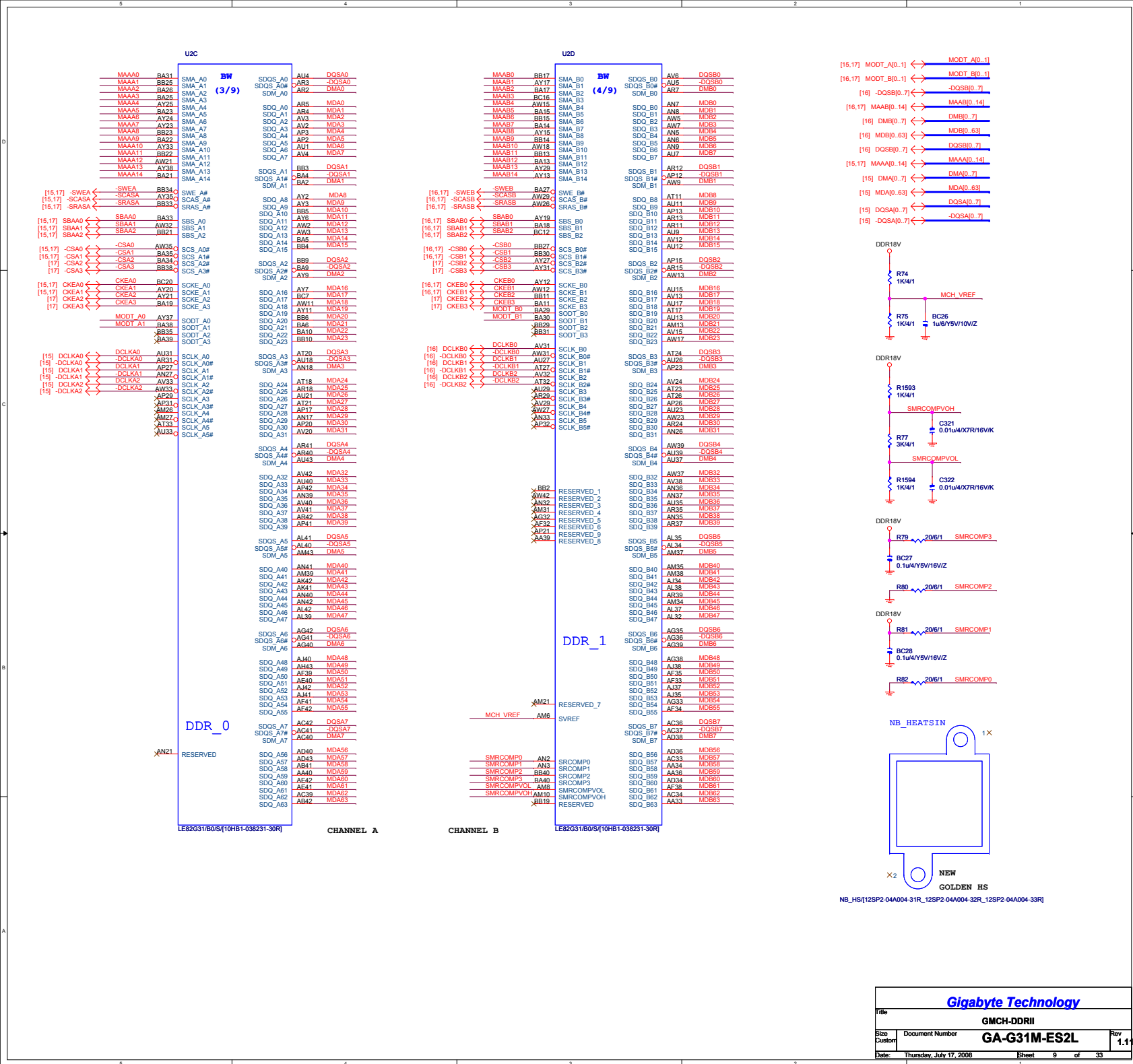
Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit

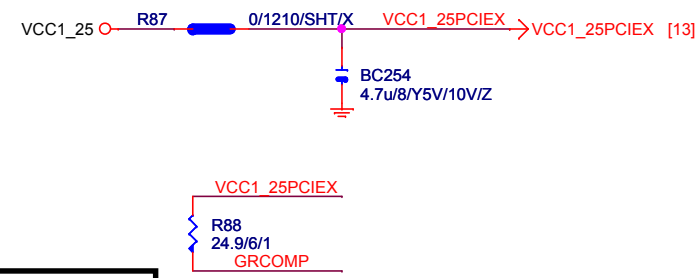
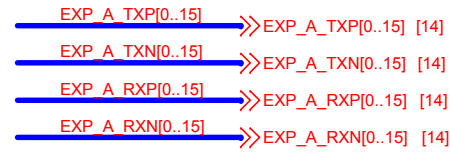
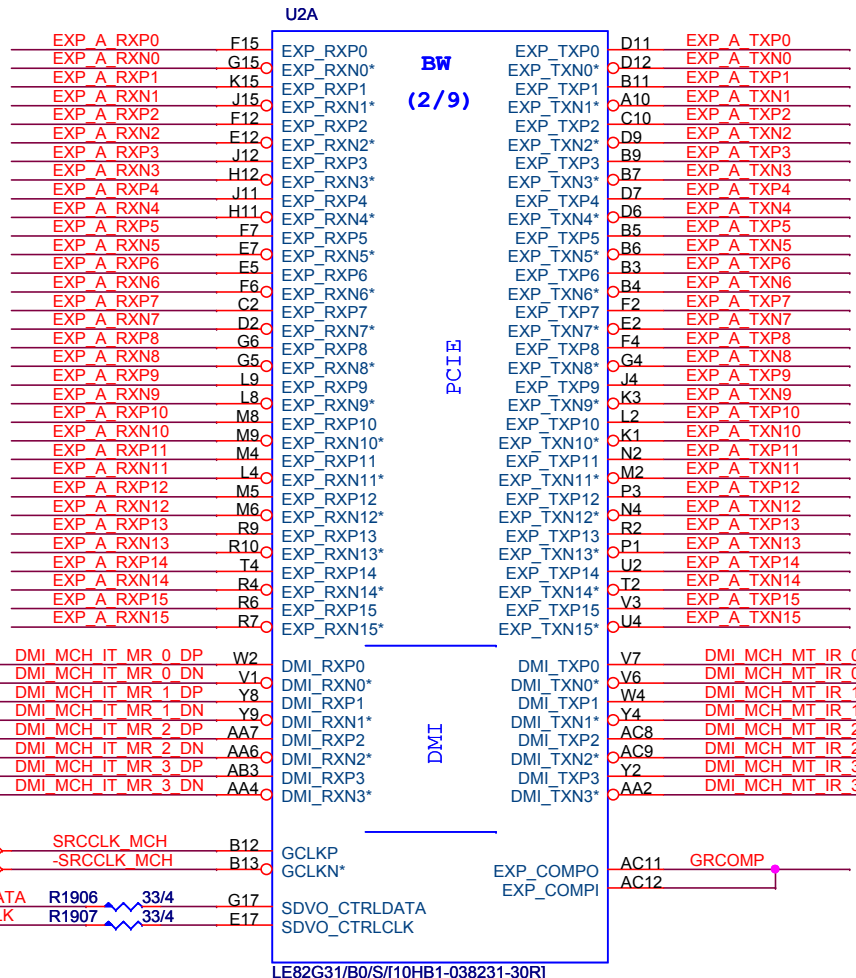


PECI:Platform Environment Control Interface

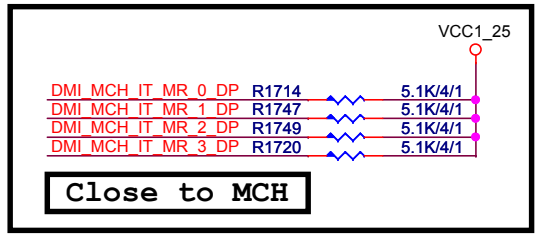
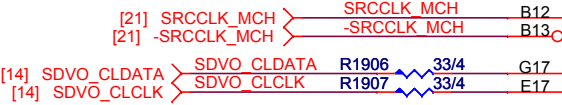
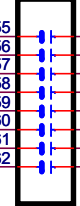


Title			
GMCH-HOST			
Size B	Document Number	GA-G31M-ES2L	Rev 1.1
Date:	Thursday, July 17, 2008	Sheet 8 of 33	





Close to MCH

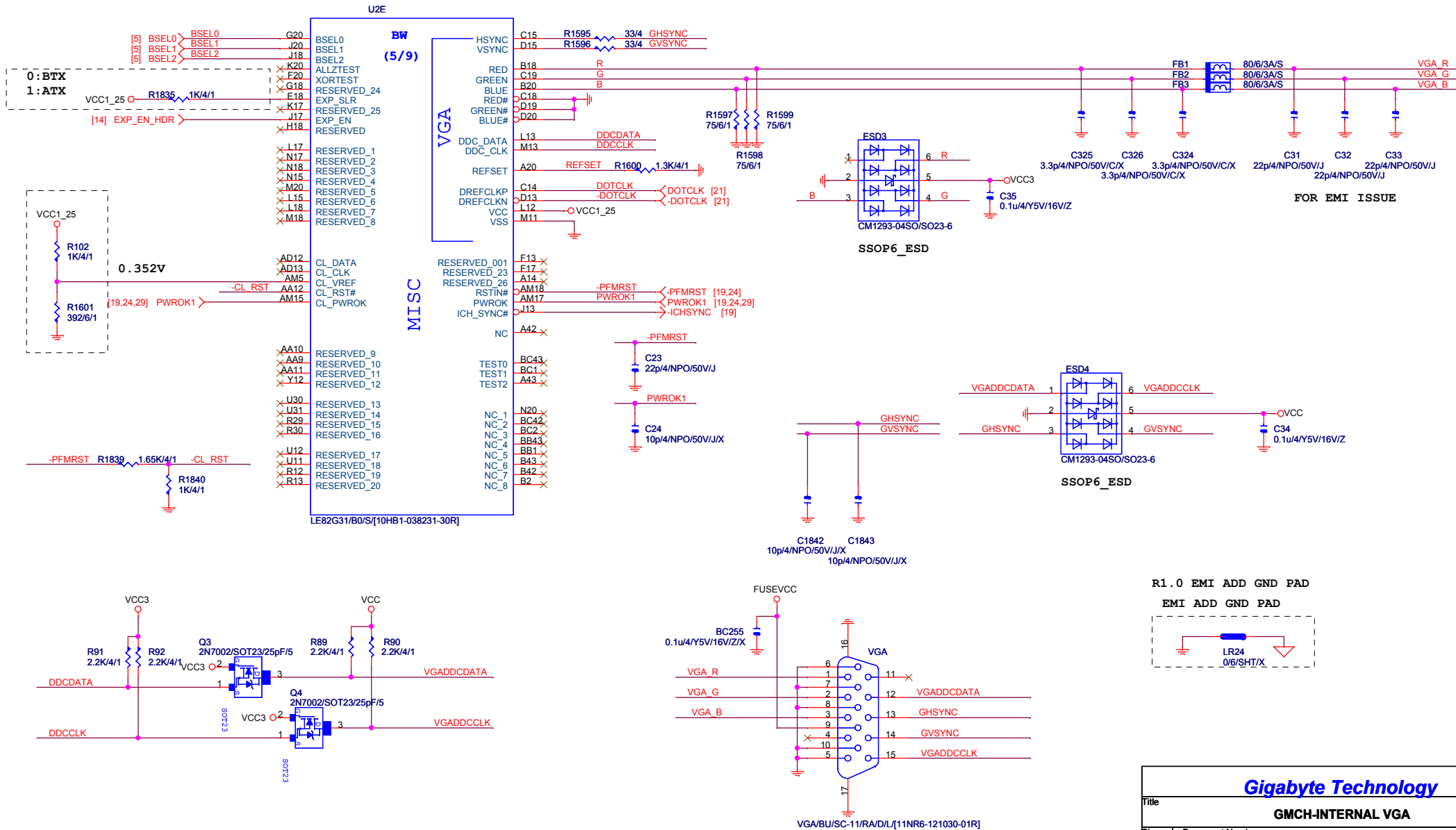


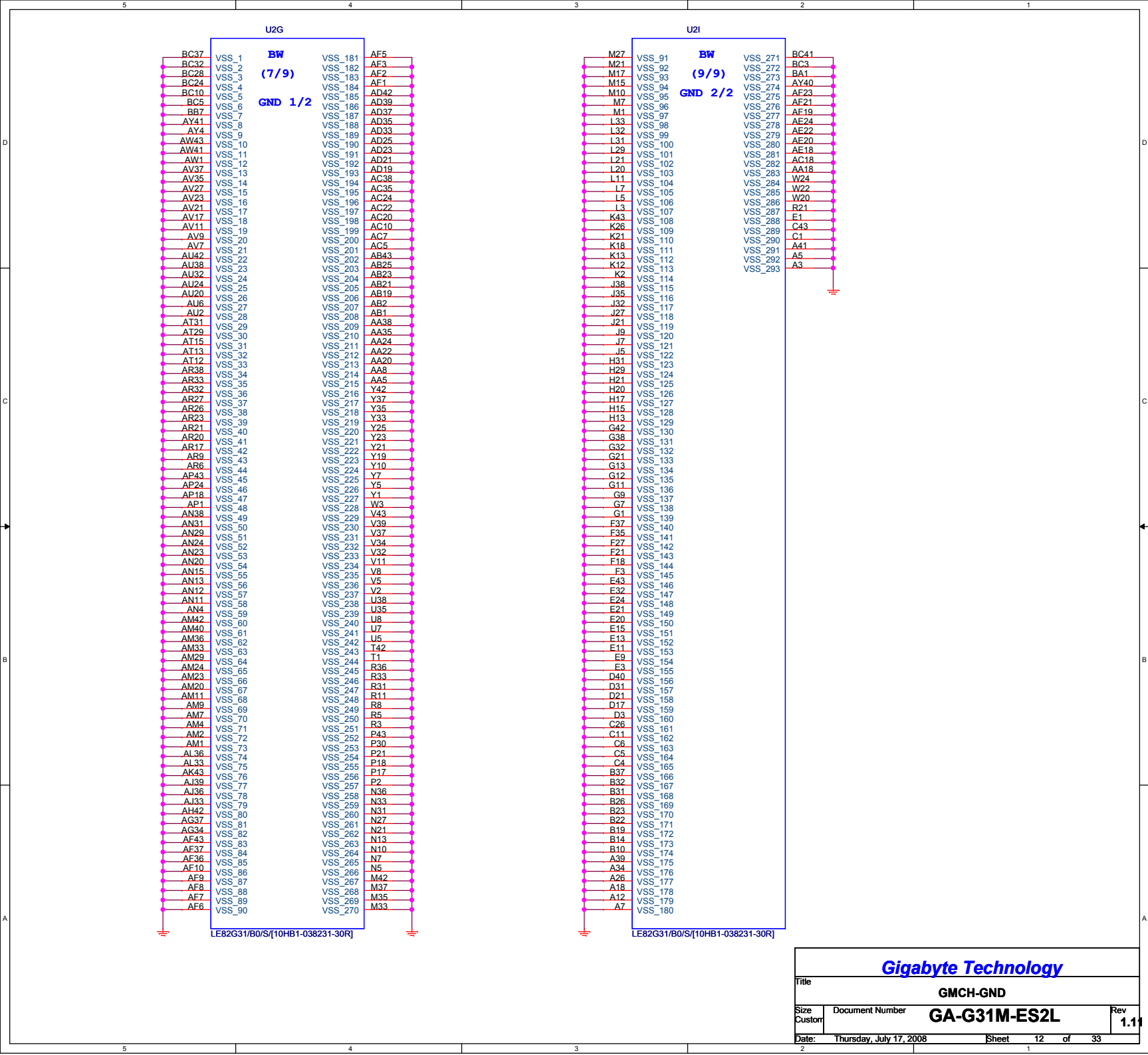
Gigabyte Technology

Title GMCH-PCI E & DMI

Size Document Number GA-G31M-ES2L Rev 1.11

Date: Thursday, July 17, 2008 Sheet 10 of 33





Gigabyte Technology

Title

GMCH-GND

Size
Custom

Document Number

GA-G31M-ES2L

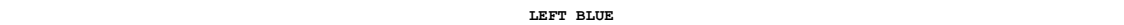
Rev
1.11


Date: Thursday, July 17, 2008

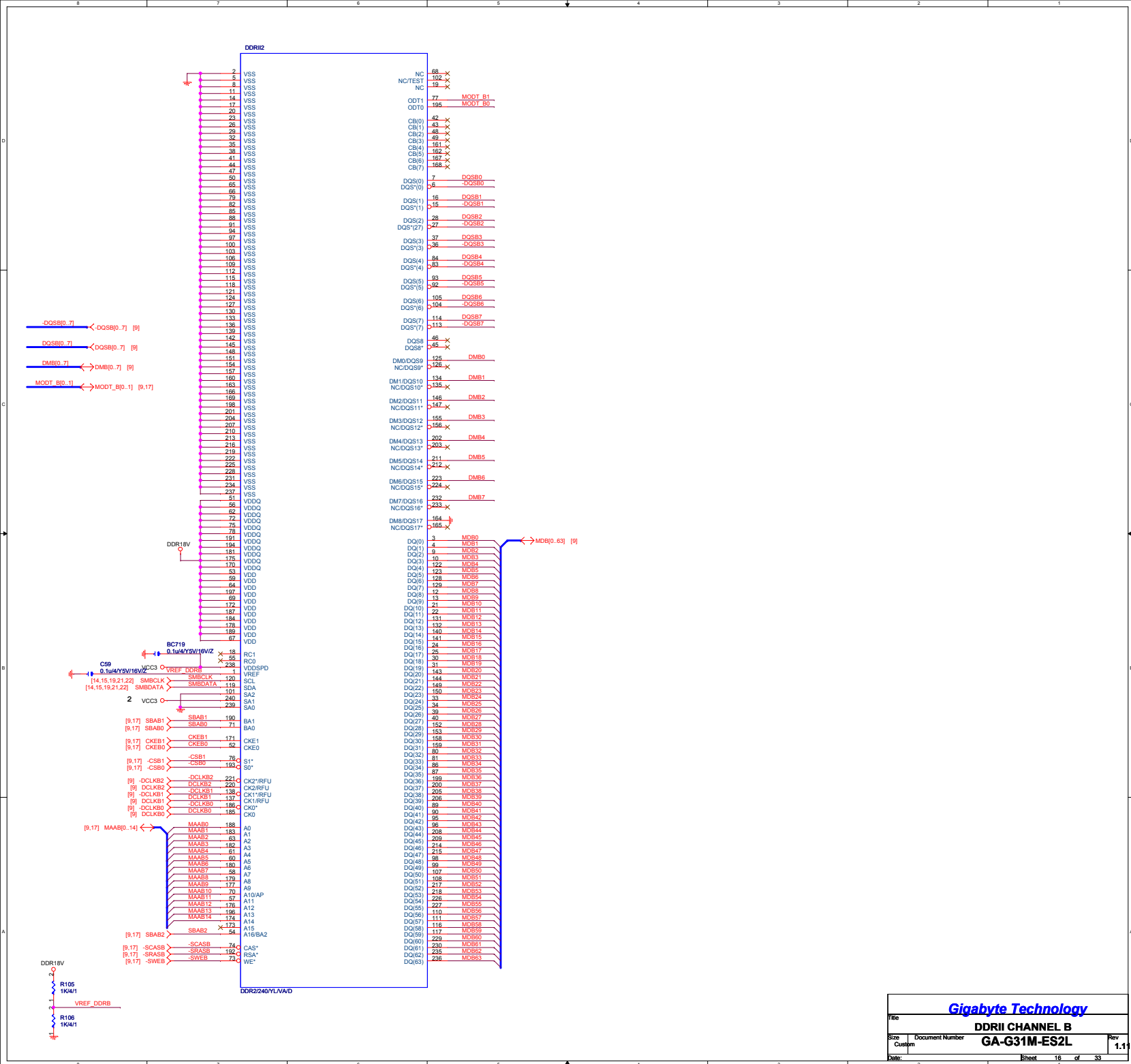
Sheet 12 of 33



EXP A TPX0	C92	1.01u4/XTR/16V/K	EXP A TPX0C
EXP A TXN0	C93	1.01u4/XTR/16V/K	EXP A TXN0C
EXP A TXP1	C94	1.01u4/XTR/16V/K	EXP A TXP1C
EXP A TXN1	C95	1.01u4/XTR/16V/K	EXP A TXN1C
EXP A TPX2	C96	1.01u4/XTR/16V/K	EXP A TPX2C
EXP A TXN2	C97	1.01u4/XTR/16V/K	EXP A TXN2C
EXP A TPX3	C98	1.01u4/XTR/16V/K	EXP A TPX3C
EXP A TXN3	C99	1.01u4/XTR/16V/K	EXP A TXN3C
EXP A TPX4	C100	1.01u4/XTR/16V/K	EXP A TPX4C
EXP A TXN4	C101	1.01u4/XTR/16V/K	EXP A TXN4C
EXP A TPX5	C102	1.01u4/XTR/16V/K	EXP A TPX5C
EXP A TXN5	C103	1.01u4/XTR/16V/K	EXP A TXN5C
EXP A TPX6	C104	1.01u4/XTR/16V/K	EXP A TPX6C
EXP A TXN6	C105	1.01u4/XTR/16V/K	EXP A TXN6C
EXP A TPX7	C106	1.01u4/XTR/16V/K	EXP A TPX7C
EXP A TXN7	C107	1.01u4/XTR/16V/K	EXP A TXN7C
EXP A TPX8	C108	1.01u4/XTR/16V/K	EXP A TPX8C
EXP A TXN8	C109	1.01u4/XTR/16V/K	EXP A TXN8C
EXP A TPX9	C110	1.01u4/XTR/16V/K	EXP A TPX9C
EXP A TXN9	C111	1.01u4/XTR/16V/K	EXP A TXN9C
EXP A TPX10	C112	1.01u4/XTR/16V/K	EXP A TPX10C
EXP A TXN10	C113	1.01u4/XTR/16V/K	EXP A TXN10C
EXP A TPX11	C114	1.01u4/XTR/16V/K	EXP A TPX11C
EXP A TXN11	C115	1.01u4/XTR/16V/K	EXP A TXN11C
EXP A TPX12	C116	1.01u4/XTR/16V/K	EXP A TPX12C
EXP A TXN12	C117	1.01u4/XTR/16V/K	EXP A TXN12C
EXP A TPX13	C118	1.01u4/XTR/16V/K	EXP A TPX13C
EXP A TXN13	C119	1.01u4/XTR/16V/K	EXP A TXN13C
EXP A TPX14	C120	1.01u4/XTR/16V/K	EXP A TPX14C
EXP A TXN14	C121	1.01u4/XTR/16V/K	EXP A TXN14C
EXP A TPX15	C122	1.01u4/XTR/16V/K	EXP A TPX15C
EXP A TXN15	C123	1.01u4/XTR/16V/K	EXP A TXN15C

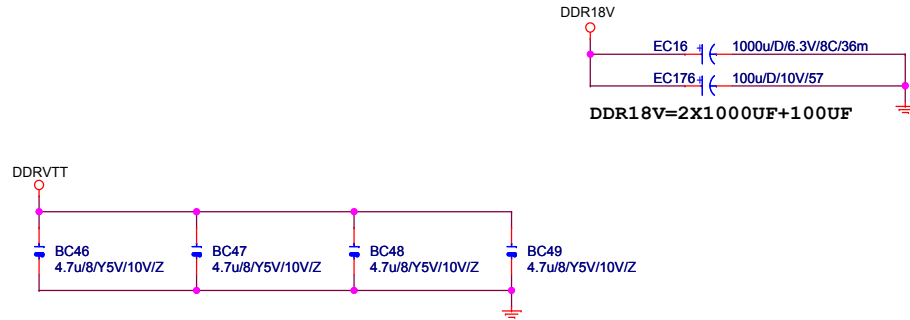


			
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PCI EXPRESS * 16			
Size	Document Number	GA-G31M-ES2L	Rev
Custom			1.1
Date:	Thursday, July 17, 2008	Sheet	14 of 33

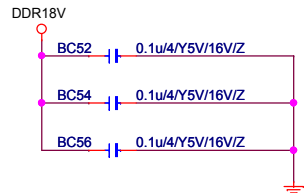


DDR TERMINATION CHANNEL A

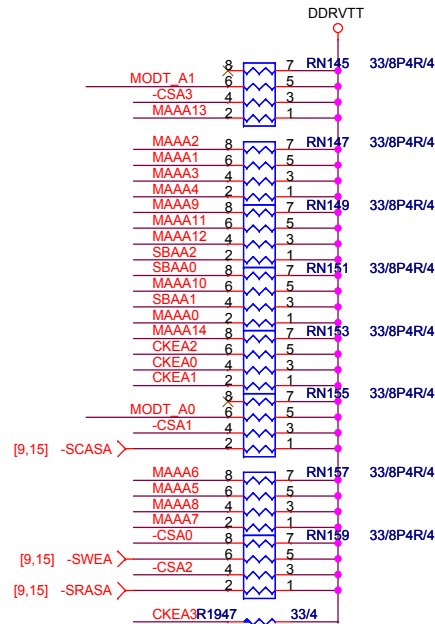
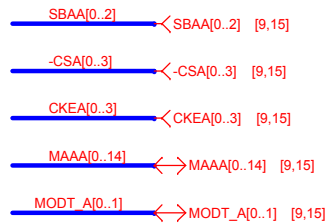
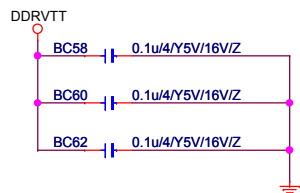
DDRVTT Decouple



DDR18V Decouple

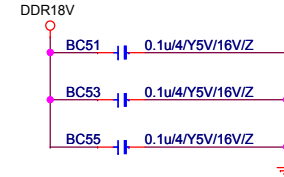


DDRVTT Decouple

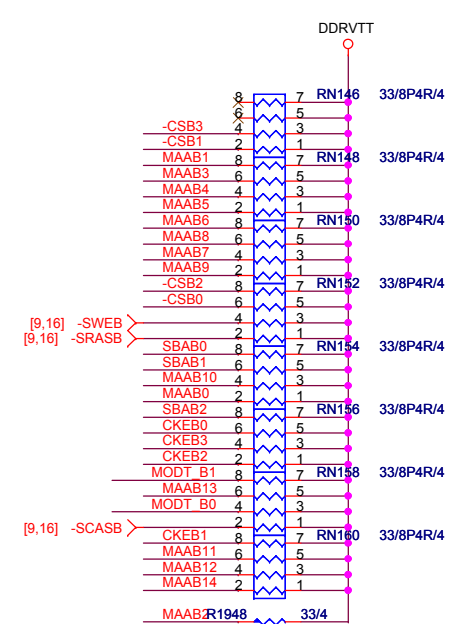
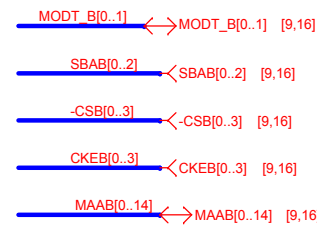
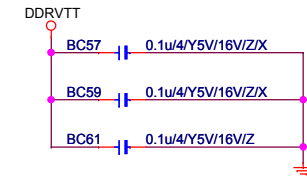


DDR TERMINATION CHANNEL B

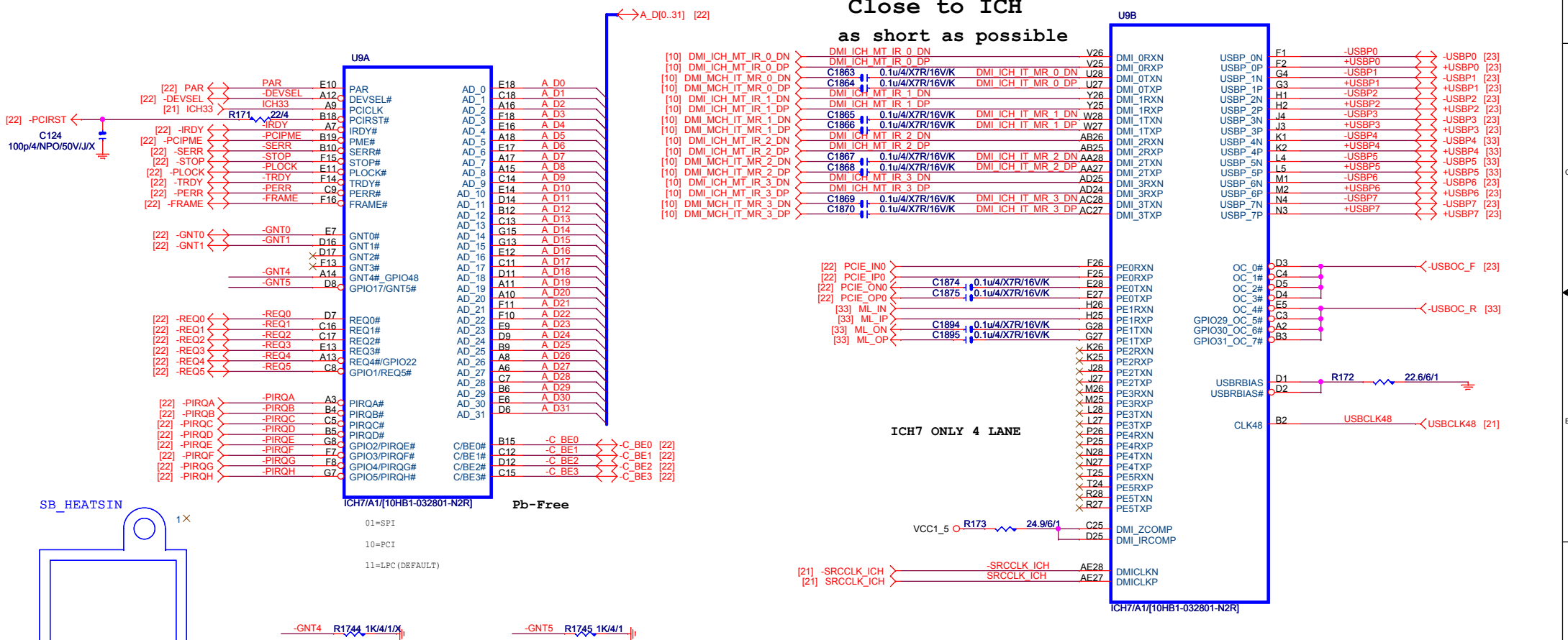
DDR18V Decouple

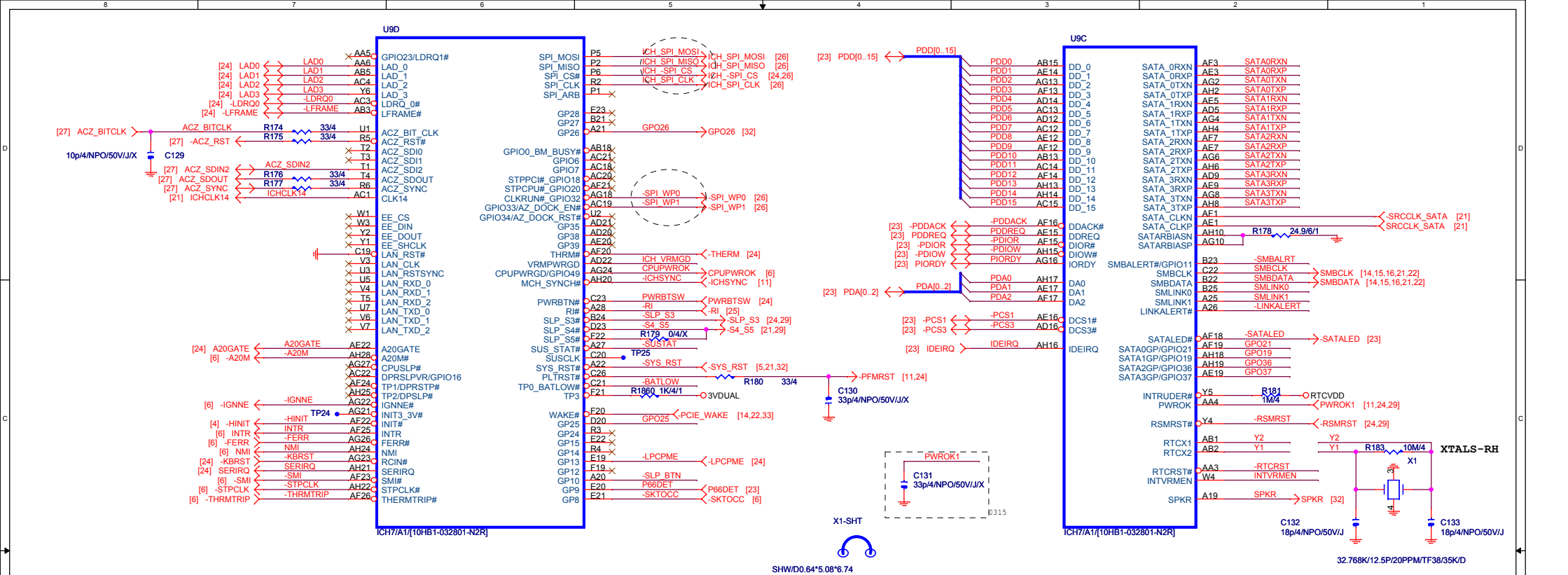


DDRVTT Decouple

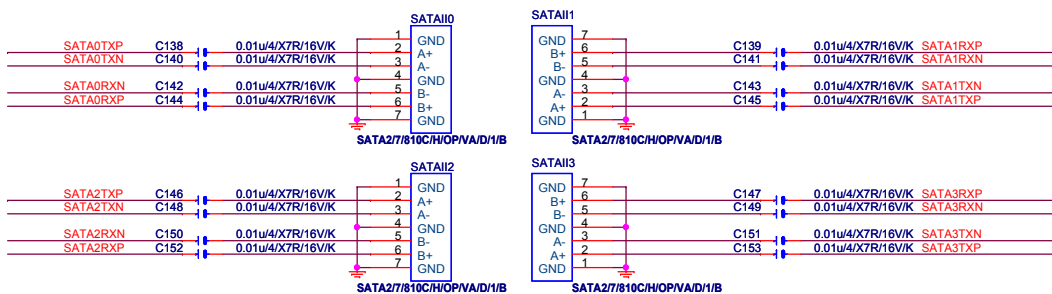
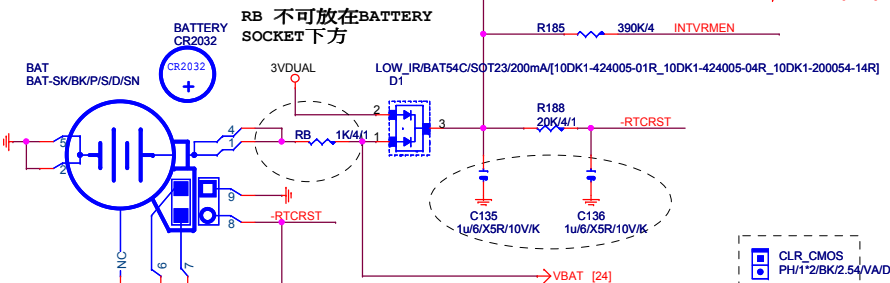


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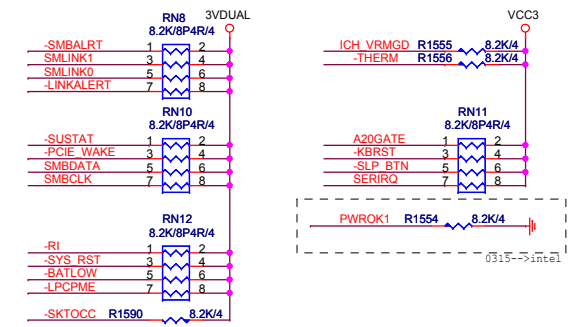




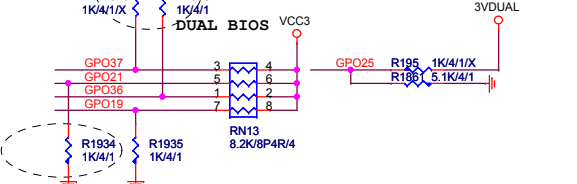
NEW TYPE: BATTERY-DUAL-4



R1.1 DES LITE DESIGN

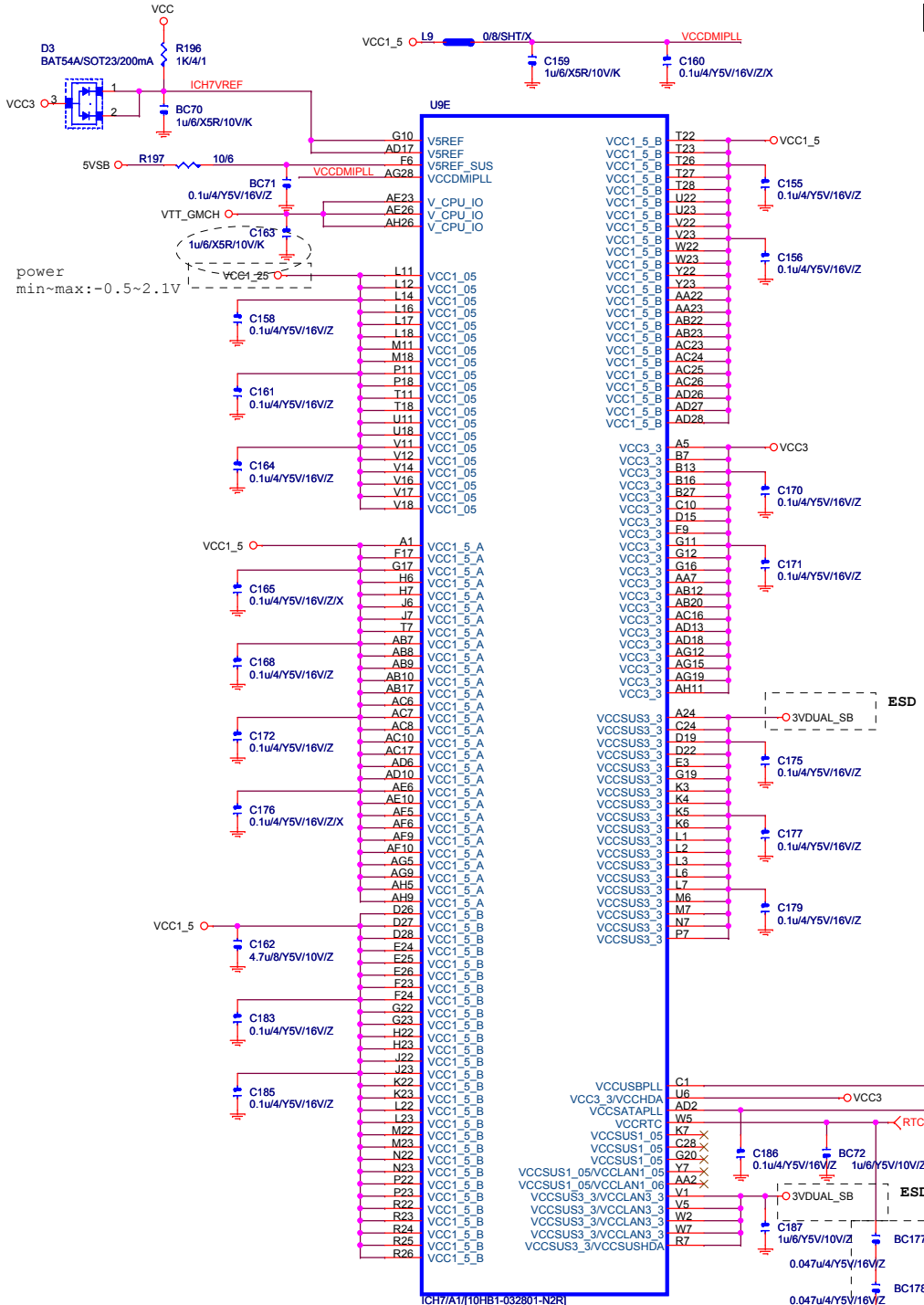


GPO25 PULL-DOWN CHECK
GPO25 (-RSMRST) LATCH時不可為LOW, 否則不開機)

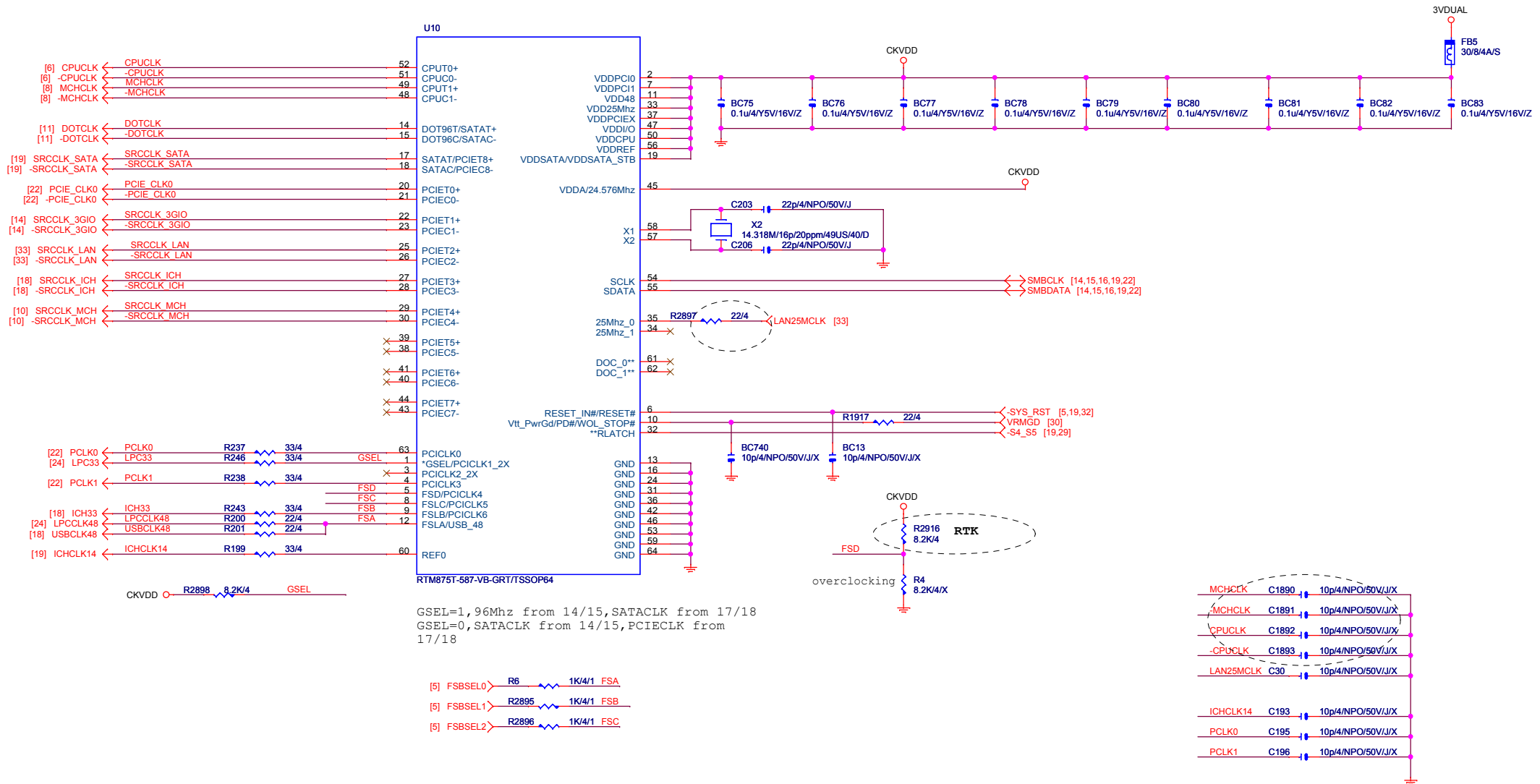


U9F			
A4	VSS1	VSS101	R14
A23	VSS2	VSS102	R15
B1	VSS3	VSS103	R16
B8	VSS4	VSS104	R17
B11	VSS5	VSS105	R18
B14	VSS6	VSS106	T8
B17	VSS7	VSS107	T12
B20	VSS8	VSS108	T13
B26	VSS9	VSS109	T14
B28	VSS10	VSS110	T15
C2	VSS11	VSS111	T16
C6	VSS12	VSS112	T17
D10	VSS13	VSS113	U4
D13	VSS14	VSS114	U13
D18	VSS15	VSS115	U14
D21	VSS16	VSS116	U15
D24	VSS17	VSS117	U16
E1	VSS18	VSS118	U17
E2	VSS19	VSS119	U24
E8	VSS20	VSS120	U25
E15	VSS21	VSS121	U26
F3	VSS22	VSS122	V2
F4	VSS23	VSS123	V13
F5	VSS24	VSS124	V15
F12	VSS25	VSS125	V16
F27	VSS26	VSS126	V27
F28	VSS27	VSS127	V28
G1	VSS28	VSS128	W6
G2	VSS29	VSS129	W24
G5	VSS30	VSS130	W25
G6	VSS31	VSS131	W26
G9	VSS32	VSS132	Y3
G14	VSS33	VSS133	Y24
G18	VSS34	VSS134	Y27
G21	VSS35	VSS135	Y28
G24	VSS36	VSS136	AA1
G25	VSS37	VSS137	AA24
G26	VSS38	VSS138	AA25
H3	VSS39	VSS139	AA26
H4	VSS40	VSS140	AB4
H24	VSS41	VSS141	AB6
H27	VSS43	VSS143	AB11
H28	VSS44	VSS144	AB14
J1	VSS45	VSS145	AB16
J5	VSS46	VSS146	AB19
J24	VSS47	VSS147	AB21
J25	VSS48	VSS148	AB24
J26	VSS49	VSS149	AB27
J26	VSS50	VSS150	AB28
K24	VSS51	VSS151	AC2
K27	VSS52	VSS152	AC5
K28	VSS53	VSS153	AC9
L13	VSS54	VSS154	AC11
L15	VSS55	VSS155	AD1
L24	VSS56	VSS156	AD3
L25	VSS57	VSS157	AD4
L26	VSS58	VSS158	AD7
M3	VSS59	VSS159	AD8
M4	VSS60	VSS160	AD11
M5	VSS61	VSS161	AD15
M12	VSS62	VSS162	AD19
M13	VSS63	VSS163	AD23
M14	VSS64	VSS164	AE2
M15	VSS65	VSS165	AE4
M16	VSS66	VSS166	AE8
M17	VSS67	VSS167	AE11
M24	VSS68	VSS168	AE13
M27	VSS69	VSS169	AE18
M28	VSS70	VSS170	AE21
N1	VSS71	VSS171	AE24
N2	VSS72	VSS172	AE2
N5	VSS73	VSS173	AF4
N6	VSS74	VSS174	AF8
N11	VSS75	VSS175	AF11
N12	VSS76	VSS176	AF27
N13	VSS77	VSS177	AF28
N14	VSS78	VSS178	AG1
N15	VSS79	VSS179	AG3
N16	VSS80	VSS180	AG7
N17	VSS81	VSS181	AG14
N18	VSS82	VSS182	AG17
N24	VSS83	VSS183	AG20
N25	VSS84	VSS184	AG26
N26	VSS85	VSS185	AH1
P3	VSS86	VSS186	AH3
P4	VSS87	VSS187	AH7
P12	VSS88	VSS188	AH12
P13	VSS89	VSS189	AH23
P14	VSS90	VSS190	AH27
P15	VSS91	VSS191	C27
P16	VSS92	VSS192	E4
P17	VSS93	VSS193	E4
P24	VSS94	VSS194	AG11
P27	VSS95		
P28	VSS96		
R1	VSS97		
R11	VSS98		
R12	VSS99		
R13	VSS100		

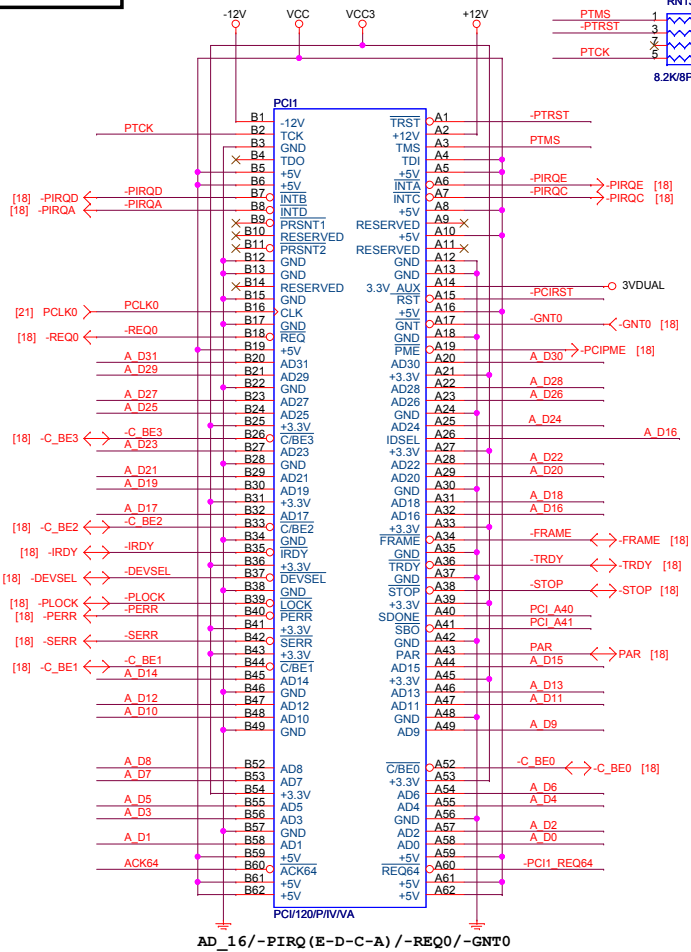
ICH7/A1/[10HB1-032801-N2R]



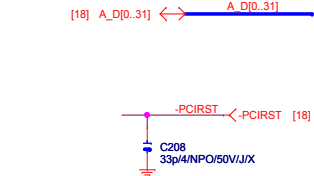
CLK GEN CK505



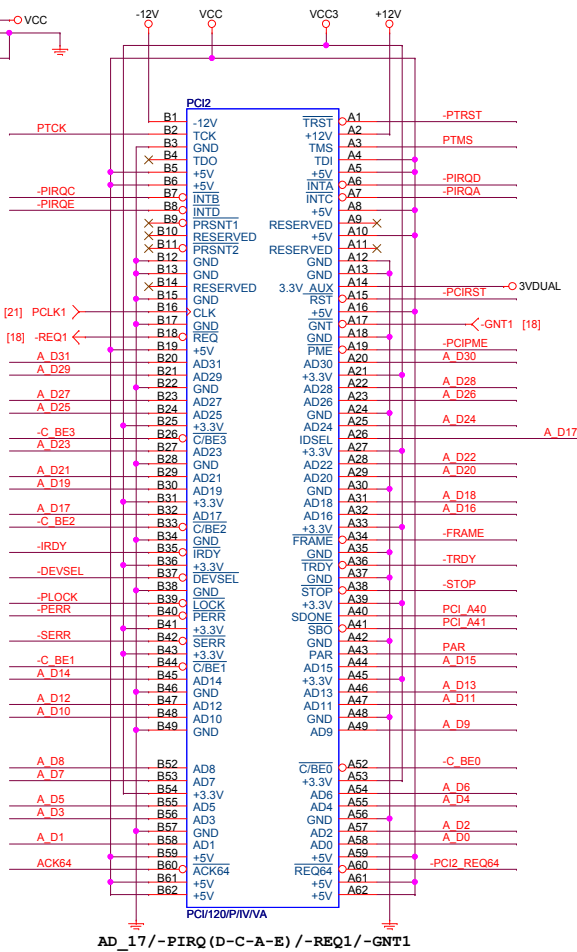
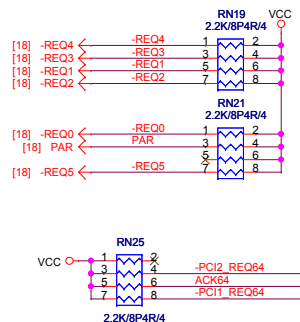
PCI1,2 SLOT



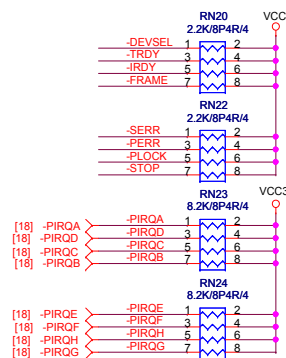
AD_16/-PIRQ(E-D-C-A)/-REQ0/-GNT0



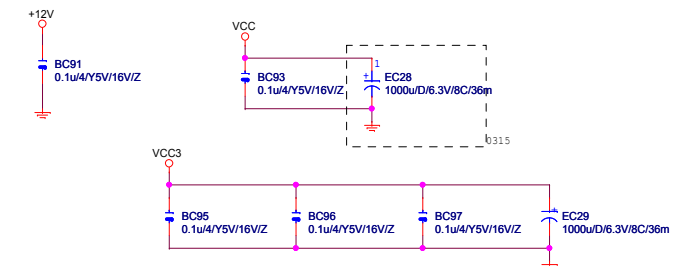
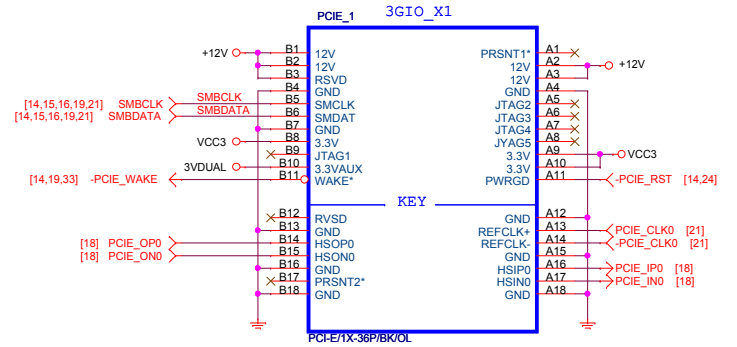
Place close to PCI1



AD_17/-PIRQ(D-C-A-E) /-REQ1/-GNT1



PCIE*1



The schematic diagram illustrates the IDE/SATA LED driver circuit. It features a -IDEACTP input signal connected to the cathode of a diode D4 (CD4148WP/1206/300mA). The anode of D4 is connected to the base of transistor Q14 (MMBT2222A/SOT23/600mA/40). The emitter of Q14 is connected to ground. The collector of Q14 is connected to the base of transistor Q15 (MMBT2222A/SOT23/600mA/40). The emitter of Q15 is connected to ground. The collector of Q15 is connected to the HDLED [32] output line. A capacitor C213 (180pF/4/NPO/50V/J/X) is connected between the output line and ground. A VCC3 supply is connected to the base of Q14 through a resistor R284 (1K/4/1) and to the base of Q15 through a resistor R285 (8.2K/4). A resistor R286 (8.2K/4) is connected between the base of Q14 and the base of Q15.

FLOPPY

VCC

RN26
470ΩP4R/V

R1815
470Ω

FDD

1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
31 32
33 34

DENSEL- [24]
INDEX- [24]
MTEA- [24]
DRVA- [24]
DIR- [24]
STEP- [24]
WDATA- [24]
WGATE- [24]
TKO- [24]
WPT- [24]
RDATA- [24]
SIDE1- [24]
DSKCHG- [24]

PH2*17K5/BK2.54/A/D

MODIFY PIN HEADER

The schematic diagram illustrates the IDE interface circuit. It features a 40-pin IDE connector connected to a BHZ*20K20/GEL/SHN/2.54V/A/D/G board. The board includes a 5V regulator (R1817, 33/4) and a -5V regulator (R1818, 470/6). The IDE pins are connected to the board's PDD0-PDD15, PDDREQ, PDIOW, PDIOR, PIORDY, PDDACK, IDEIRQ, PDA1, PDA0, PCS1, and IDEACTP. The board also has a P66DET pin connected to a C1849 capacitor (0.047uF/4V/5V/16V/Z).

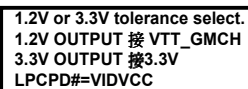
The schematic diagram illustrates the internal components of the USB1 module. On the left, the 'FRONT USB1' view shows the connection of USB signals to the ESD1 protection diode array (CM1293-04SO/SO23-6) and the BC780 fuse (0.1u/4Y5V/16V/Z). The right side shows the 'FUSEVCC1' view, detailing the connection of the fuse to the F_USB1 fuse block (PHI2*5K9/YL/2.54/N/A/D) and the FUSEVCC1 pin.

[illegible]

The schematic diagram illustrates the power supply and signal conditioning for the USB to RS-485 module. It features two input power sources: a 5V DUAL supply and a 160MILS supply. The 5V DUAL supply is connected to a 240MILS supply through a 150K/4 resistor (R321). The 160MILS supply is connected to a 270K/4 resistor (R322). Both resistors are connected to a common point labeled -USBOC_F [18]. The 240MILS supply is also connected to a 150K/4 resistor (R321) and a 270K/4 resistor (R322). The 150K/4 resistor is connected to a 270K/4 resistor (R322). The 270K/4 resistor is connected to a common point labeled -USBOC_F [18]. The 240MILS supply is also connected to a 150K/4 resistor (R321) and a 270K/4 resistor (R322). The 150K/4 resistor is connected to a 270K/4 resistor (R322). The 270K/4 resistor is connected to a common point labeled -USBOC_F [18].

[illegible]

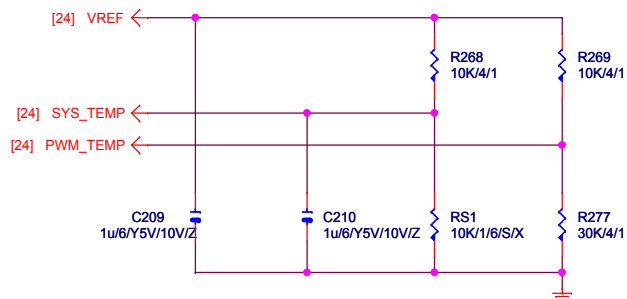
DEFAULT 50%



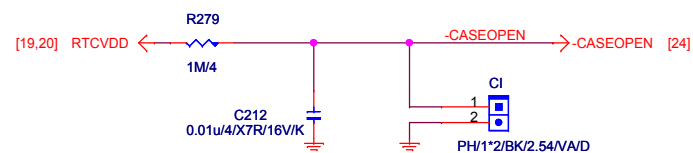
[26] -SIO_SPI_CS1 << 0/4 R412 CEB_N

[26] -SIO_SPI_CS0 << 0/4 R404 -RST_BTN

TEMP H/W MONITOR

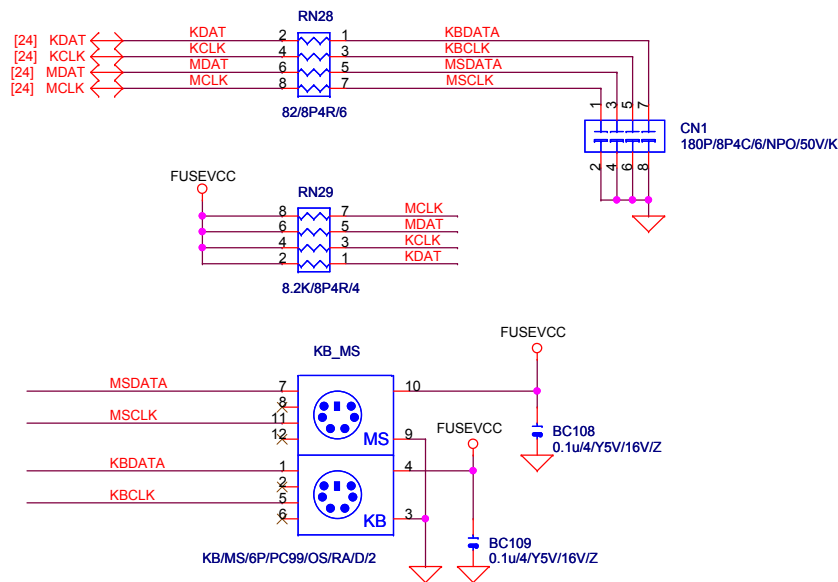


CASE OPEN

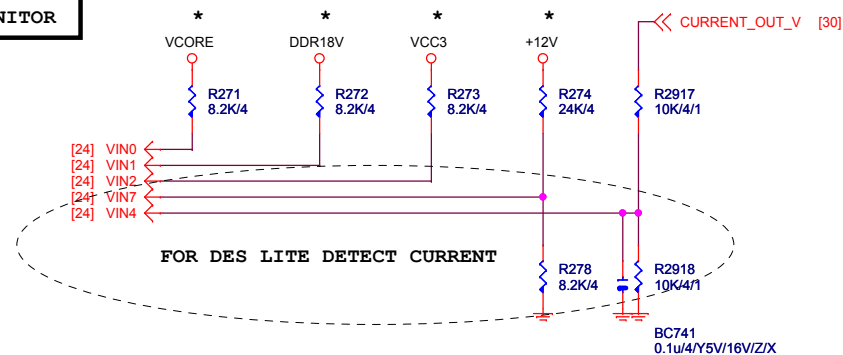


Case Open Circuits

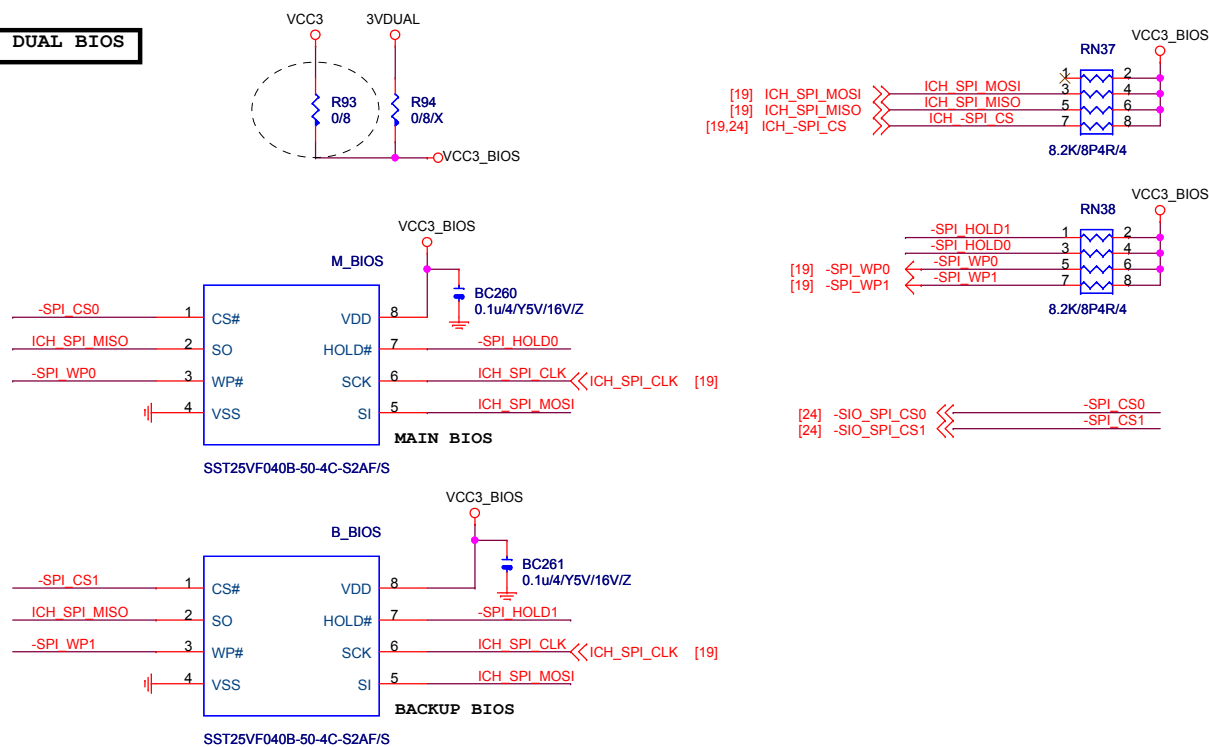
KB/MS



VOLTAGE-- H/W MONITOR



DUAL BIOS

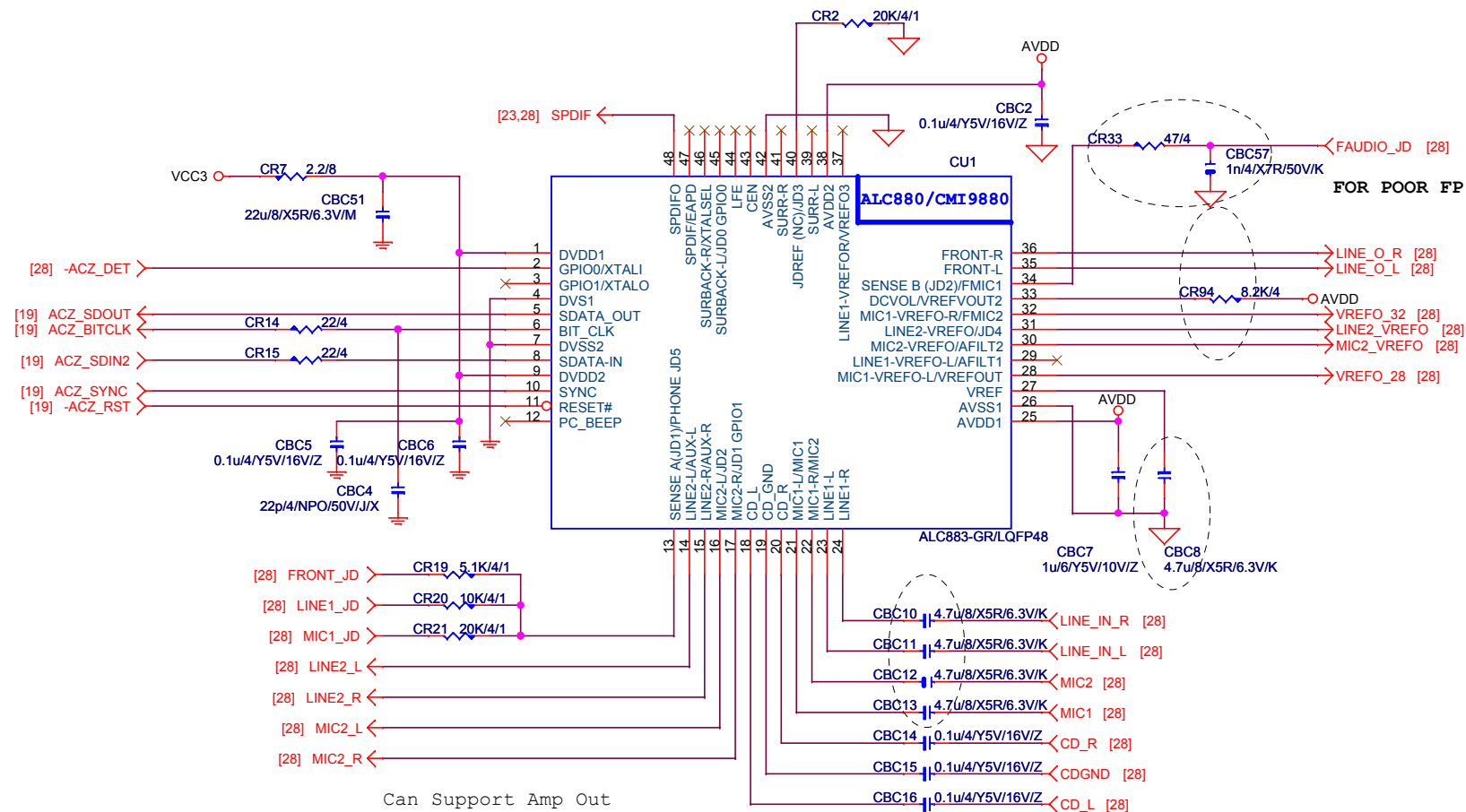


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HW-MONITOR/CI/KB/MS/BIOS

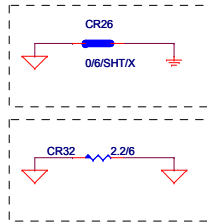
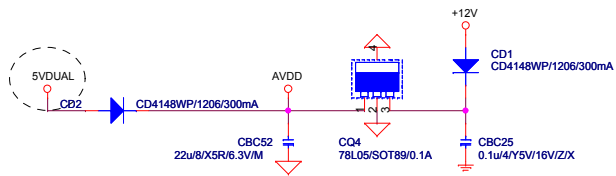
Size Custom	Document Number GA-G31M-ES2L	Rev 1.1
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Date:	Thursday, July 17, 2008	Sheet	26	of	33
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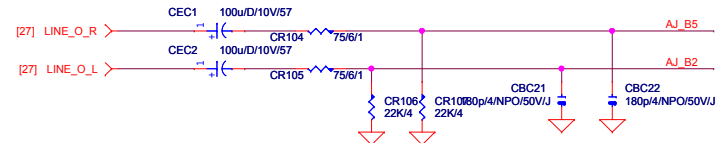
**Gigabyte Technology**

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AZALIA ALC883		
Size	Document Number	Rev
Custom	GA-G31M-ES2L	1.1
Date:	Thursday, July 17, 2008	Sheet 27 of 33

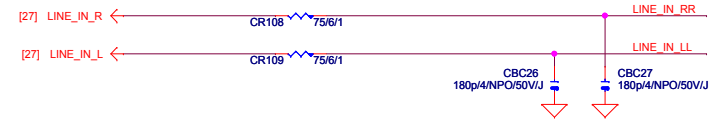
CODEC POWER/EMI PAD



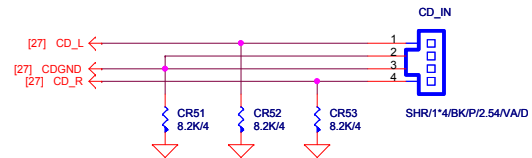
LINE-OUT



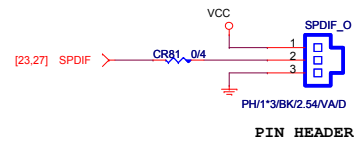
LINE-IN



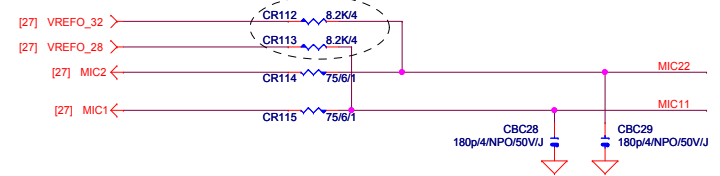
CD IN



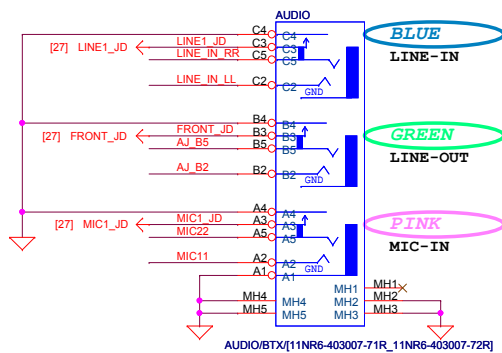
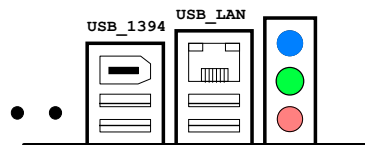
SPDIF IN



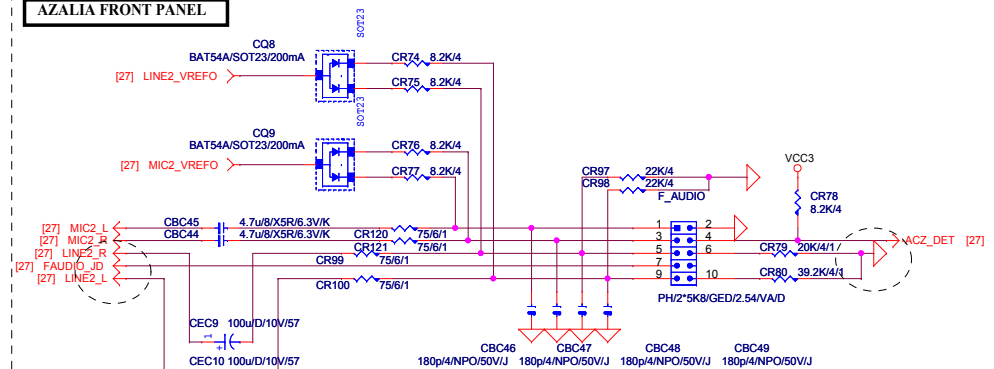
MIC-IN



AZALIA JACK



AZALIA FRONT PANEL



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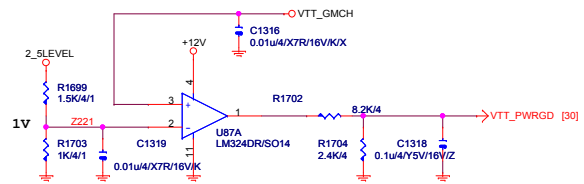
AUDIO JACK

GA-G31M-ES2L

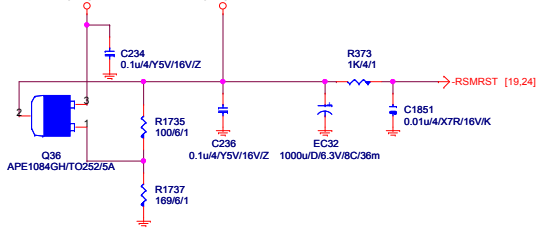
Rev 1.11

Date: Thursday, July 17, 2008 Sheet 28 of 33

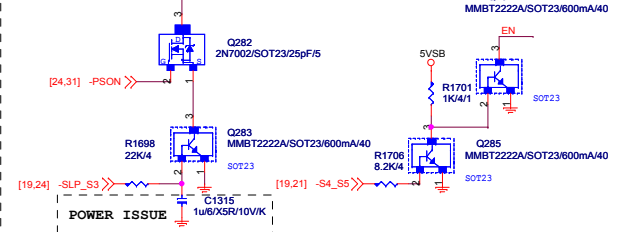
VTT_PWRGD



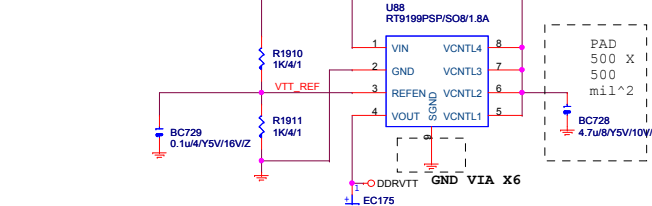
3VDUAL



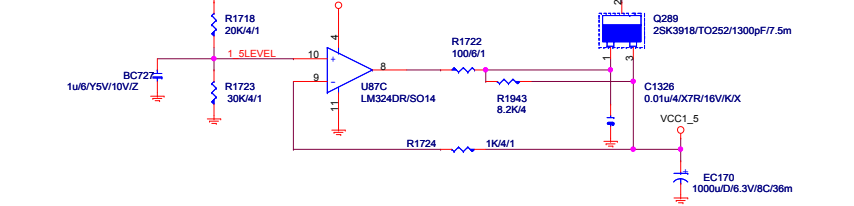
PWR_SEQ



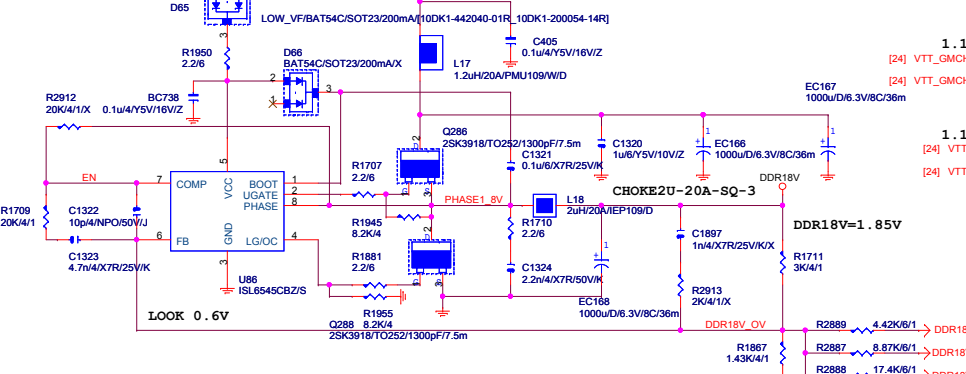
DDR_VTT



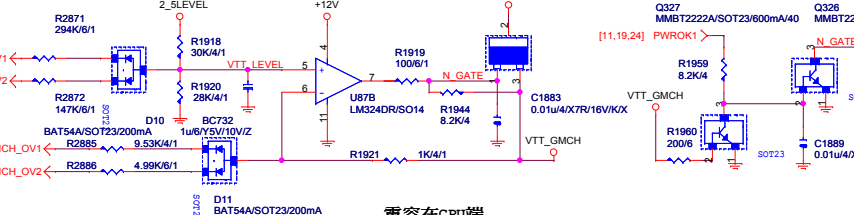
VCC1_5



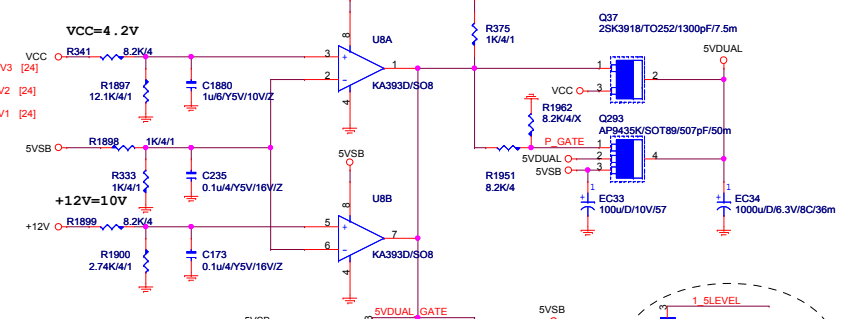
DDR18V



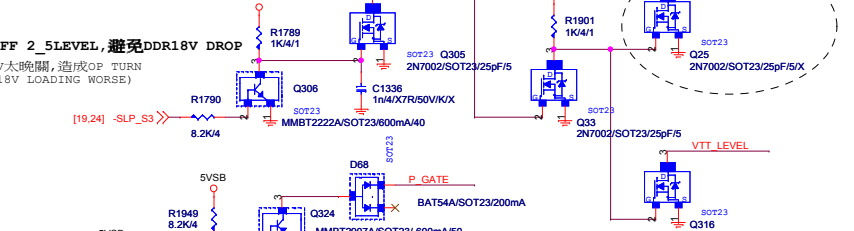
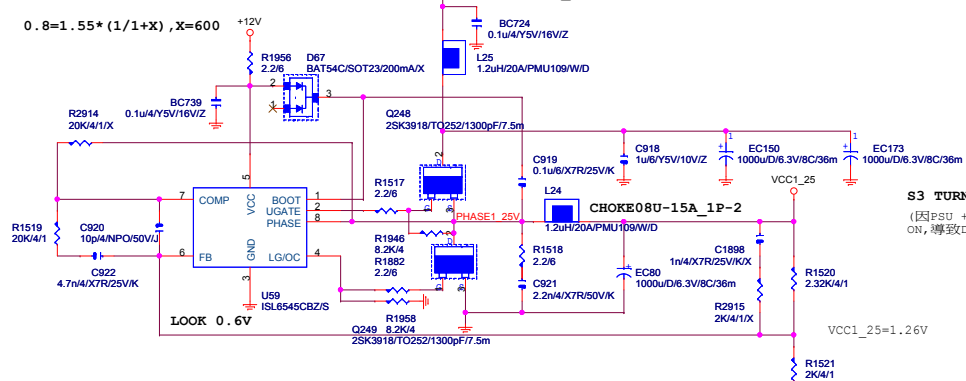
VTT_GMCH



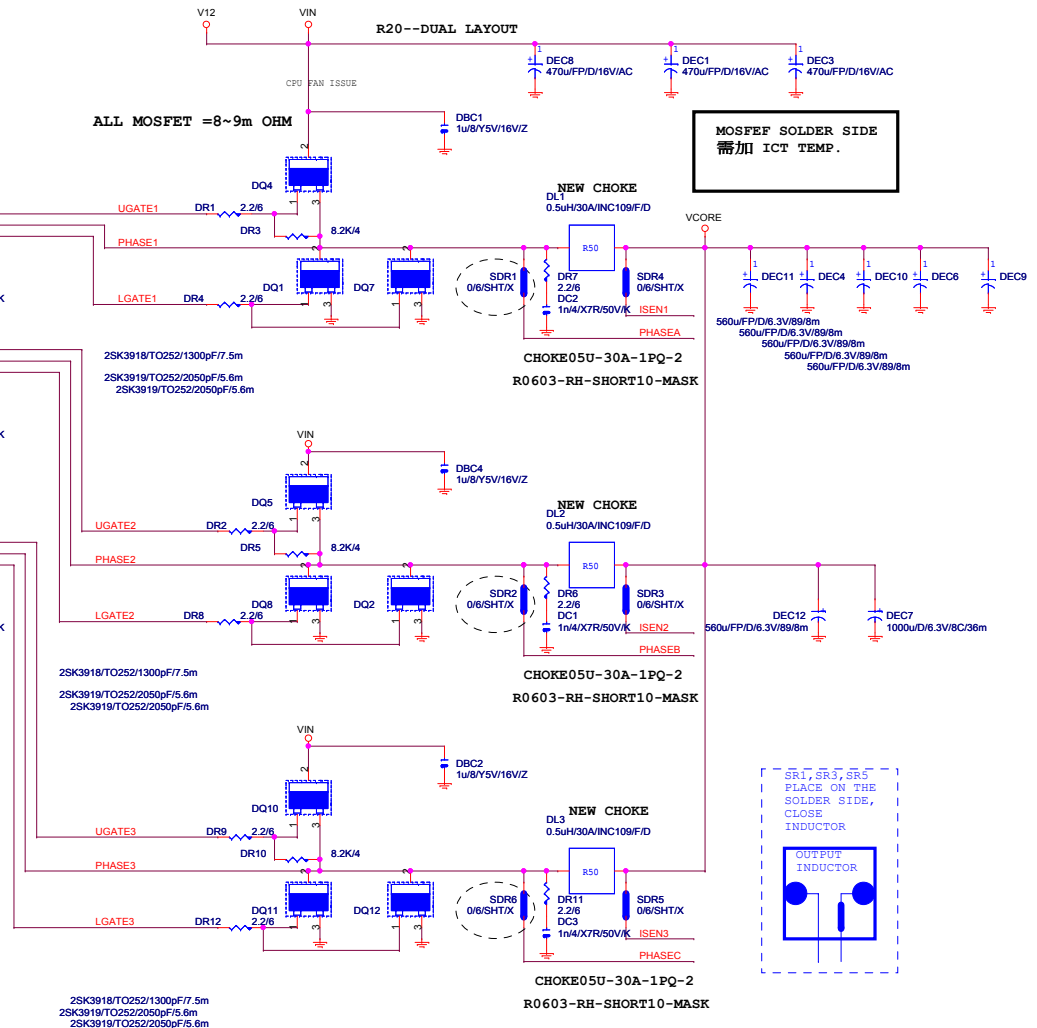
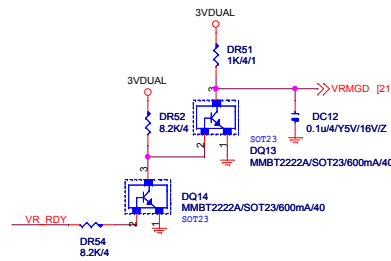
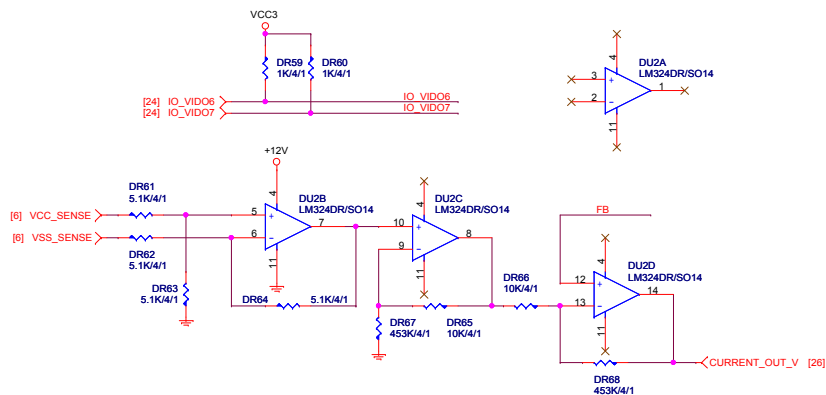
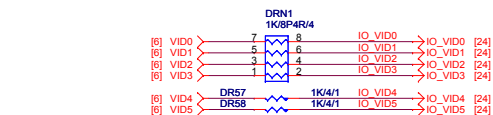
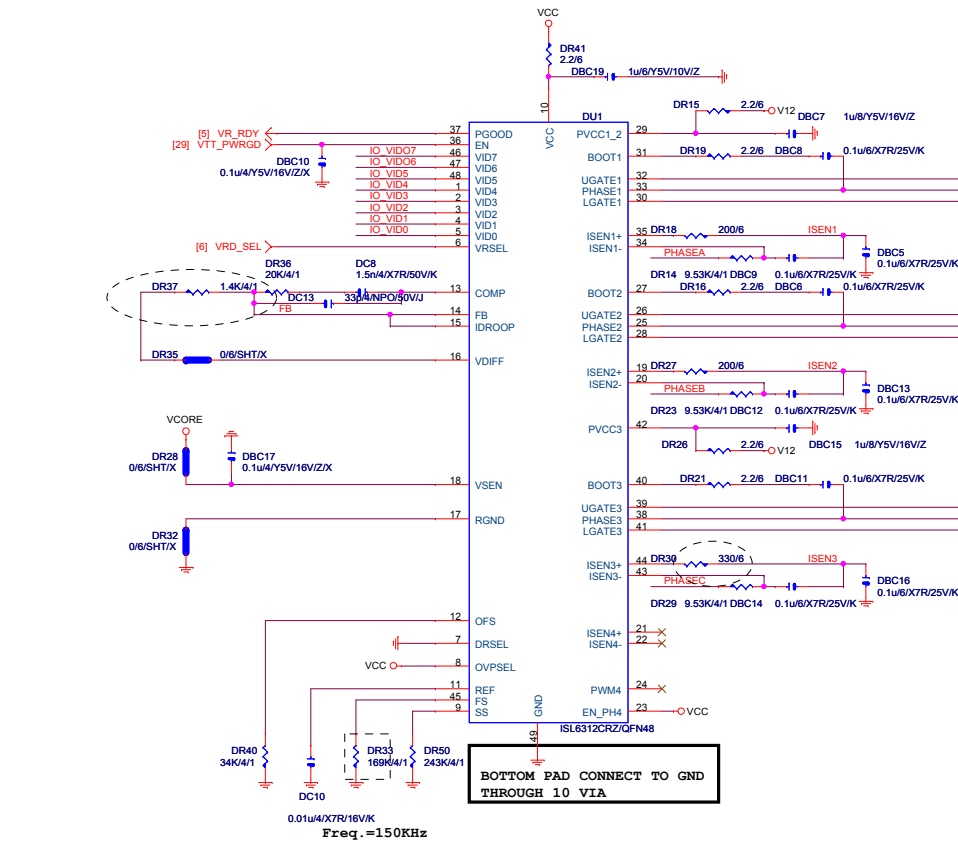
5VDUAL



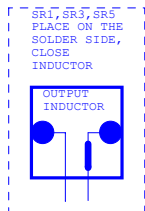
VCC1_25



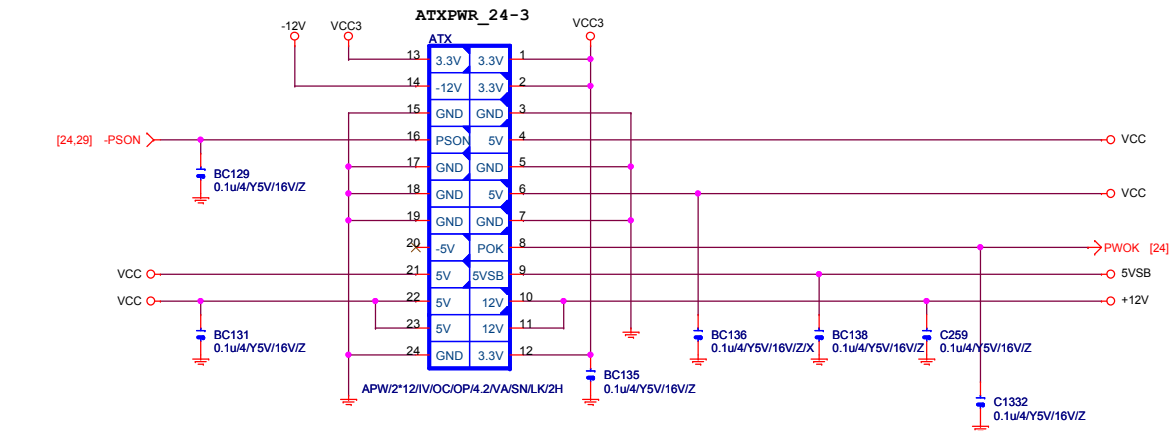
S3 TURN OFF 2_5LEVEL, 避免DDR18V DROP
(因PSU +12V太晚關, 造成OP TURN ON, 導致DDR18V LOADING WORSE)



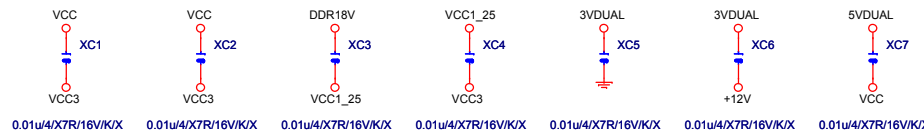
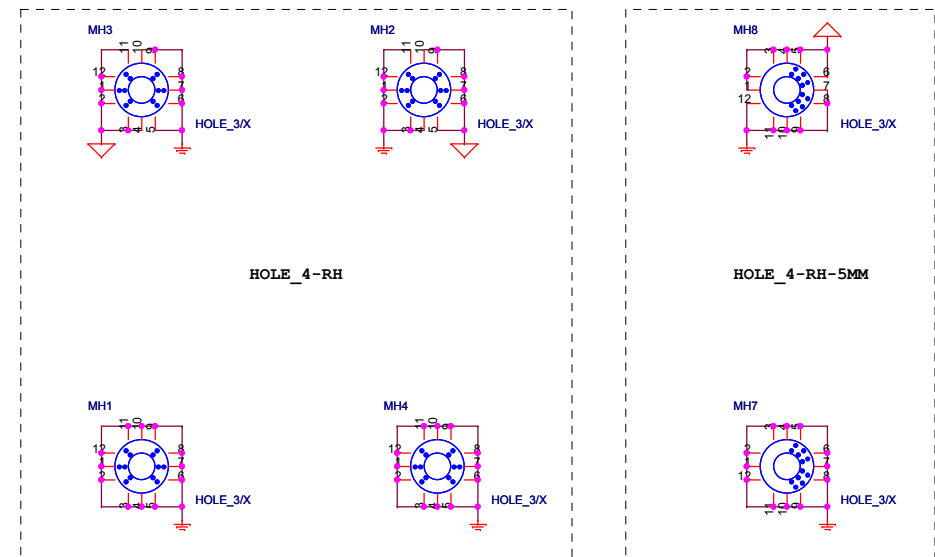
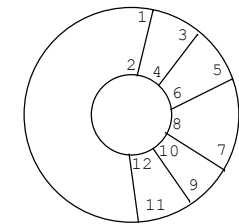
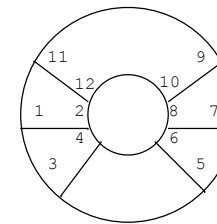
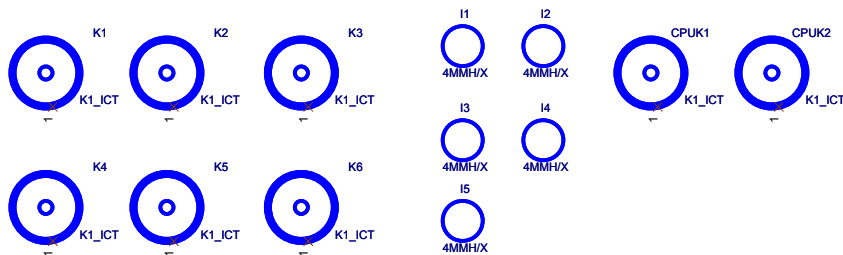
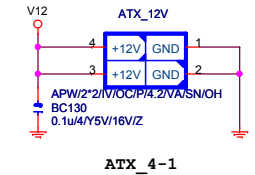
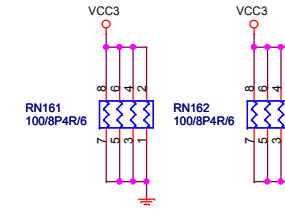
MOSFET SOLDER SIDE
需加 ICT TEMP.



ATX POWER CONNECTOR



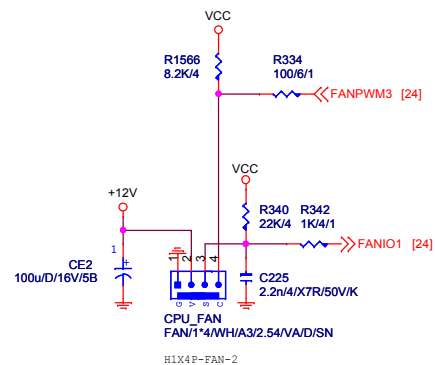
FIX PWR AcBel (ATX-400C-A2ADB)



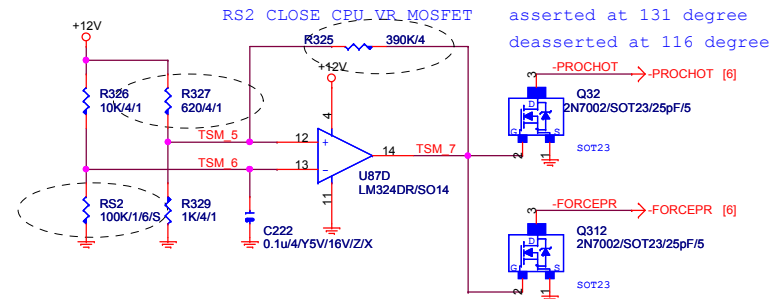
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Title		
ATX POWER CONNECTOR		
Size B	Document Number	GA-G31M-ES2L
Date:	Thursday, July 17, 2008	Sheet 31 of 33
		Rev 1.11

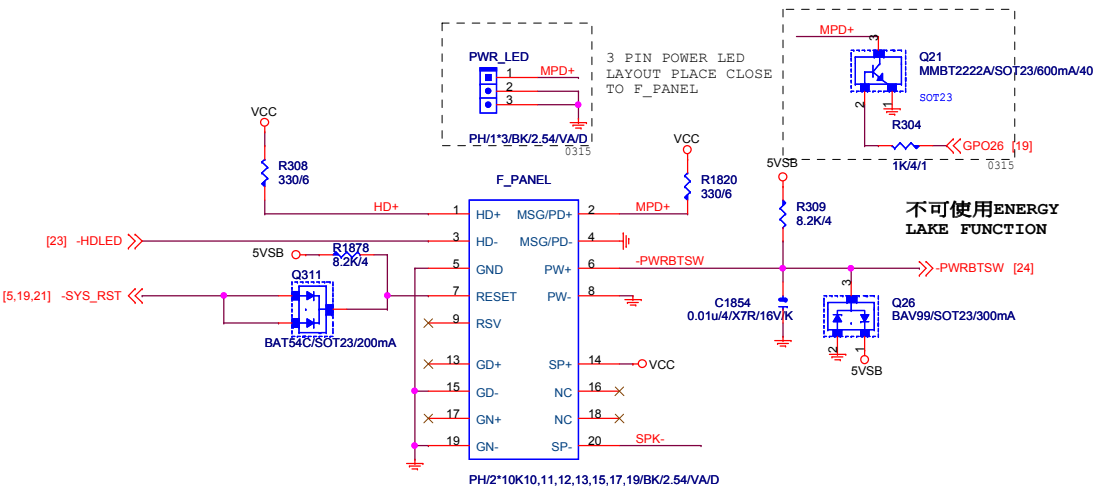
CPU SMART FAN SMART FAN



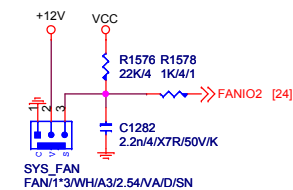
PROCESSOR HOT



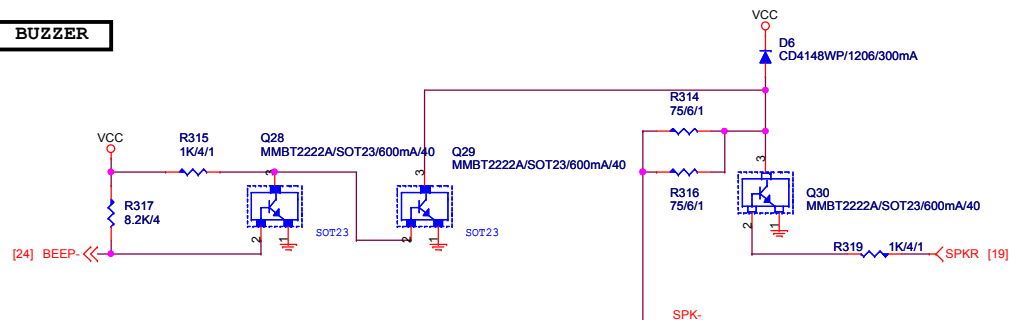
INTEL FRONT PANEL



SYS_FAN



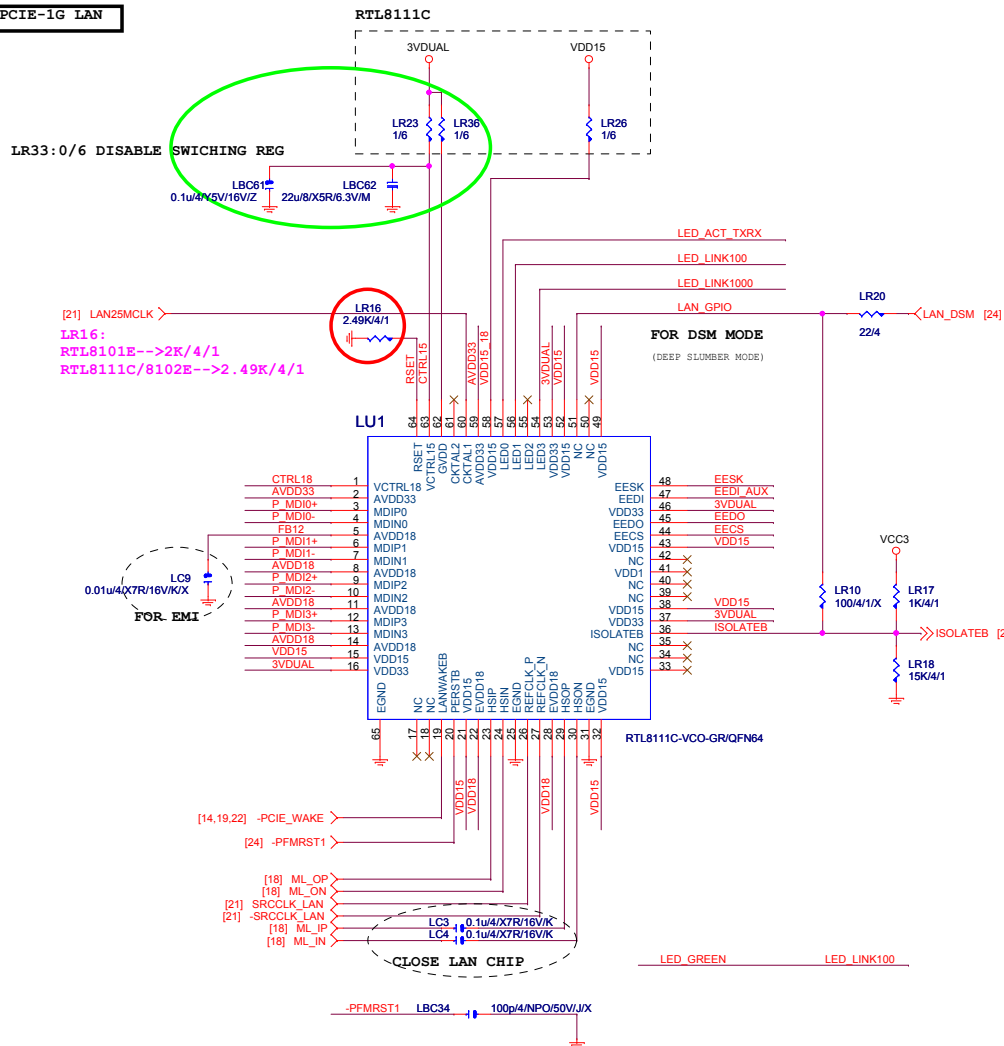
BUZZER



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Title	FRONT PANEL		Rev
Size	Custom	Document Number	1.11
Date:	Thursday, July 17, 2008	Sheet	32 of 33
GA-G31M-ES2L			

PCIE-1G LAN

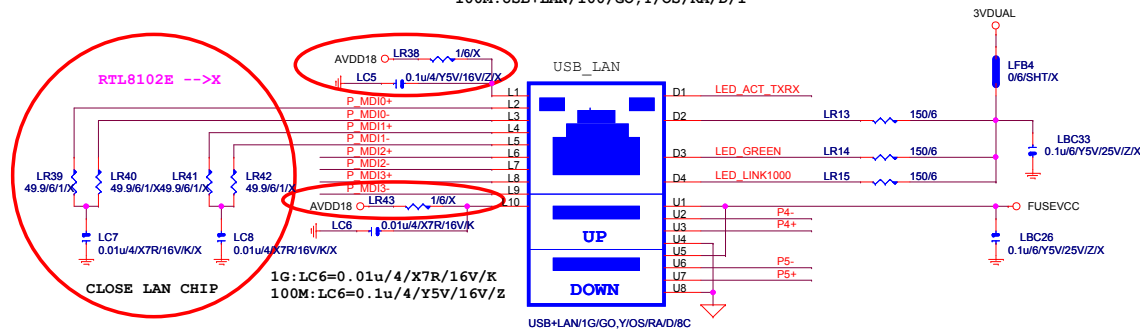


USB_LAN CONNECTOR

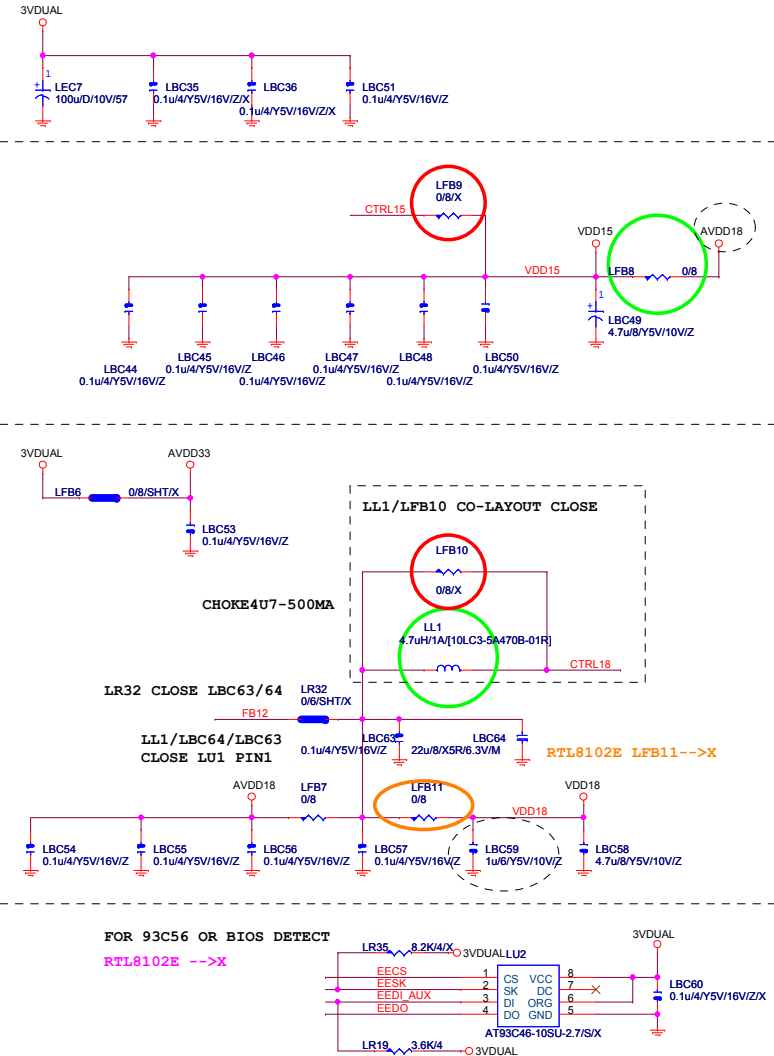
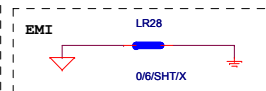
```
RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8102E:LC5/LC6-->O
RTL8111C:LC6-->O
```

```
RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
```

```
1G   :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
```



USB LAN



Gigabyte Technology

REALTEK RTL8111C/8101E

Size	Document Number	GA-G31M-ES2L	Rev
Custom			1.11

Date: Thursday, July 17, 2008 Sheet 33 of 33